

Integration and Testing of a Digital Transceiver for a Dual Frequency, Pulse-Doppler Radar

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Abstract

This dissertation focuses on the development of a digital transceiver system for a dual-band, polarimetric radar, which is to form part of the NeXtRAD multistatic radar. NeXtRAD is being developed as an instrument for research into the behaviour of clutter and targets as observed by multistatic radars. The Pentek Cobalt model 71621 software defined radio interface was procured for use as the digital transceiver in the system. The goal was to develop the software needed to use this product as the digital transceiver in a prototype version of the NeXtRAD active node, and to ensure that it could be readily integrated with other subsystems in the final system. The active node is essentially a monostatic pulse-doppler radar. Laboratory tests of the transceiver showed that it was possible to generate and digitize pulsed waveforms at a 125 MHz intermediate frequency which is used by the existing receiver exciter in the system. After extensive laboratory testing and development, phase coherent waveform generation and multichannel digitization was achieved. A low transmit power version of the active node was constructed and tested at both operating frequencies. Equipment used in the testing and development of the digital transceiver included laboratory signal generators, spectrum analyzers and oscilloscopes. The digital transceiver was able to function at pulse repetition rates exceeding 2 kHz, with a single transmit channel and three receive channels active. The low-powered monostatic prototype system was constructed to test the digital transceiver using a receiver exciter subsystem, RF amplifiers and antennas. This prototype radar was used to take measurements of targets at ranges below 300 m and successfully detected reflections from large structures. Cars and pedestrian traffic were detected by their doppler shifts at both L- and X-band frequencies. The detection of moving and stationary targets confirmed the suitability of the digital transceiver for use in the envisioned multistatic radar system.

Declaration

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Date: August 31, 2016

Dane Paul du Plessis

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Nomenclature

ADC	– Analogue to digital converter, also denoted A/D
ASIC	– Application specific integrated circuit.
ATP	– Application test procedure.
AWG	– Arbitrary Waveform Generator.
CLI	– Command Line Interface.
DAC	– Digital to analogue converter, also denoted D/A
DDC	– Digital down-converter
DSP	– Digital signal processing.
DT	– Digital transceiver.
DUC	– Digital up-converter
FDU	– Frequency distribution unit
FFT	– Fast Fourier transform
FPGA	– Field Programmable Gate Array
GPSDO	– Global positioning system disciplined oscillator
IF	– Intermediate Frequency
LFM	– Linear Frequency Modulation
LO	– Local oscillator
LVPECL	– Low Voltage Positive Emitter Coupled Logic
MSPS	– Mega-samples per second
NCO	– Numerically controlled oscillator
PRF	– Pulse repetition frequency
PRI	– Pulse repetition interval
REX	– Receiver Exciter
RF	– Radio Frequency
SBD	– System Block Diagram
SDR	– Software Defined Radio
XMC	– Switched Mezzanine Card, an IEEE P1386.1 standard

Chapter 1

Introduction

This dissertation details the work done in the development of a digital transceiver system for NeXtRAD, which is a multistatic, dual-frequency, dual-polarization radar. This research instrument has been designed to capture multistatic radar data on sea clutter. NeXtRAD expands on the capabilities of its predecessor, NetRAD, which was jointly developed by UCL and UCT to study target and clutter behaviour as observed by multistatic radar.

Radars systems have been instrumental in shaping the recent history of the world. These systems detect targets at ranges far greater than visible light or sound waves will permit. The outcome of many major conflicts from the early twentieth century have been profoundly affected by this technology. On a more positive note, the peacetime applications of radar have greatly benefited humanity. Commercial aviation relies heavily on radar systems to ensure the safety of thousands of people every day. Space based radars have proved useful in measuring movements of a few centimeters in ground level, helping seismologists understand and predict earthquakes. Vegetation growth can be monitored by airborne or space-based radar systems. They are also indispensable tools in modern meteorology, enabling weather forecasts. Oceangoing vessels depend on radar for navigation and safety. Automotive radars are becoming an increasingly important feature in modern vehicles, and will only become more so, as driverless cars begin to proliferate. In many important human endeavours, these instruments have been and will continue to be of great service to humankind.

To build an effective radar is a considerable technical challenge, requiring the best available in microwave and digital signal processing technology. Radar systems draw on many different fields of knowledge, including electrical and computer engineering, radio and microwave frequency technology, analogue and digital signal processing, statistical analysis, to name a few.

Radars are the appropriate instruments to use when detecting targets in darkness through atmospheric moisture at large ranges. The laws of physics dictate the electromagnetic frequencies that can be used for detection of targets under these conditions, usually ranging from a few millimeters to tens of meters. Visible light has much shorter wavelengths and attenuates too rapidly to be much use in cloud

or fog. Longer wavelengths in to the microwave region of the spectrum exhibit optical scattering when scattered from targets with physical dimensions many times a wavelength. These are attenuated by the atmosphere, but not nearly as much as visible light. Longer wavelengths suffer less attenuation and can even penetrate the ground, however targets with dimensions much smaller than a wavelength behave like isotropic scatterers, which can make identification difficult. Dual-frequency radars such as NeXtRAD get around the limitations of using a single wavelength; they gather more information from targets from the different scattering modes of the two frequencies.

Pulse-doppler radars in monostatic configuration work by illuminating a target with pulsed radio waves and detecting energy scattered by the targets back to the receiver. Distance to the target is then calculated from the time of flight, and the target is in the direction of the antenna's main beam (ignoring sidelobes). The phase difference between consecutive received pulses can be used to calculate the target's doppler shift, which is related to its radial velocity. Monostatic configurations, where distance between transmitter and receiver is small compared with the range to target, are the most commonly fielded type of radar system. In bistatic or multistatic radar topologies the separation between receiver and transmitter is much larger - comparable to target range, as depicted in Figure 2.1. Multistatic systems have one or more transmitters and several receivers, are categorized as multi-input, multi-output (MIMO) systems [1]. One potential advantage of such configurations is immediately obvious when the aspect-dependent scattering pattern of a target is considered; with more than one receiver surrounding the scatterer, it is more likely that one of them will intercept the energy reflected from the transmitter. Of course there could be more than one transmitter. Such a network of cooperative transmitters and sensors have the potential to achieve better performance than monostatic configurations. There is also the possibility of improved stealth capability in military applications if there are several passive nodes.

The increasing availability of high-quality microwave components which are cheaper and more sensitive than before make the development of networked radar feasible. Highly stable crystal oscillators, or perhaps atomic clocks, make coherent radar processing possible with spatially distributed receivers and transmitters using separate reference oscillators. Much work remains to be done in developing and understanding networked radar systems.

1.1 Background and Research Motivation

The development of the digital transceivers that form part of NeXtRAD is the focus of this dissertation. There is significant scope for new research into the multistatic perspective of sea clutter. Useful multistatic, dual-band, polarimetric radar data is rare in the private domain for two reasons: (1) military radar data for these measurements is likely to be classified, and (2) the measurements are difficult to make given the complexity of multistatic systems. There is, therefore, a need to develop an instru-

ment for gathering multistatic sea clutter data. Some factors affecting clutter and target measurements include the multistatic geometry, frequency and polarization of the transmitted pulses, sea state, and many others which are not yet well understood.

The NeXtRAD instrument will consist of three radar stations (nodes) arranged along a coastline as in Figure 2.1. The middle node is active, the other two passive. The nodes focus their antennas (of 10° azimuth beamwidth) cooperatively on a target area on the sea surface. NeXtRAD is a pulse-doppler radar which will operate in both X- and L-band, with dual-polarization capability in each frequency band. The radar is fully polarimetric on receive in X-band, and L-band signals can be transmitted or received in either horizontal or vertical polarization, making six modes of operation possible. NeXtRAD will offer a platform for taking dual-frequency, dual-polarization, multistatic measurements which provide new data for statistical analysis of sea clutter. Deeper understanding of sea clutter can be used to develop better detection and tracking of targets hidden in sea clutter. There is significant scope for new research using this kind of radar data.

1.2 Objectives

This research project contributes to the broader objective of building a multistatic radar system by focusing primarily on the development of the digital transceiver, i.e., the digital backend of NeXtRAD. System specifications have predetermined requirements for the transceiver. To meet these user requirements, a Pentek Model 71620 digital transceiver module, the also called the “Cobalt” card was procured. This is a high-speed, multi-channel data converter well suited to software defined radio applications.

The project objective was to develop control software for the Cobalt module to enable seamless integration with neighbouring subsystems in the active node of NeXtRAD, as shown in Figure 1.1. These subsystems included:

- a dual-band, multi-channel receiver exciter (REX) developed by Reutech Radar Systems [2],
- a Timing Control Unit (TCU) based on the Rhino board, implemented by Burger [3],
- a Frequency Distribution Unit (FDU) which provides a stable time and frequency reference, developed by Sandenberg and Inggs [4].

1.2.1 Project Scope

The user requirements for the digital transceiver (DT) included inter alia

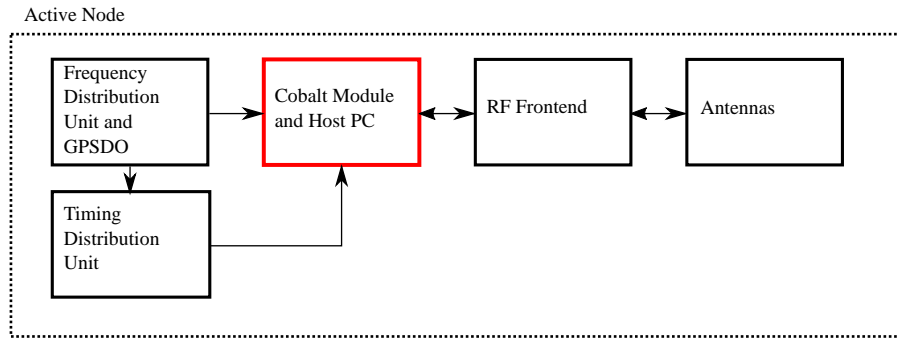


Figure 1.1: A simplified system block diagram of the NeXtRAD active node, the software defined radio transceiver module bordered in red demarcates the project scope.

Waveform generation – The DT would need to generate the required analogue transmit pulse at an intermediate frequency compatible with REX.

Waveform digitization – The DT was required to receive and digitize three separate analogue receive channels at the intermediate frequency from REX. Data was to be acquired in contiguous blocks and appended to a single file per receive channel.

Triggering and phase stability – The DT would need to synchronize its internal oscillators to a 10 MHz reference clock common to the entire system from the FDU, and accept an external trigger for the initialization of transmit/digitization from the TCU.

The above list of user requirements have been thoroughly specified in Section 2.2.1. Software tools created by Pentek purchased with the Cobalt module were required to develop the programs for meeting these objectives.

1.2.2 Exclusions

Areas of responsibility excluded from the project objectives were the following:

- Configuring and testing the REX, TCU, or FDU subsystems.
- Building a prototype mono- or bistatic radar system.
- Developing system control software not directly related to configuring and operating the digital transceiver.

Although a prototype radar *was* built, the express purpose of this assembly was to provide confirmation that the digital transceiver and its controlling software satisfied user requirements given in Section 2.2.1.

1.3 Dissertation Overview

1.3.1 System Overview

To put the function of the digital transceiver into perspective, Chapter 2 gives a broad overview of the NeXtRAD system. The role of the digital transceiver is made clear by explaining the basic operating principles of NeXtRAD as a complete system. The NeXtRAD system parameters are given in Table 2.1, and high-level diagram of the system in Figure 2.2 shows the main components in the active and one of the passive nodes of the radar, together with the command and control computer which links the nodes via a wireless network.

The active node is then brought into focus in Figure 2.3. This diagram shows the active node's subsystem and how they interconnect, with emphasis on the Cobalt digital transceiver. The interconnections between the Cobalt, REX, TCU, and FDU are briefly explained, as these give context to the operational requirements on the Cobalt module.

The user requirements for the digital transceiver are then spelled out in Section 2.2.1. These user requirements were set in place before the development work was undertaken and so were subject to a level of interpretation, depending on the hardware constraints of the Cobalt module. Essentially the Cobalt is required to interface with the receiver exciter to transmit and digitize radar signals on a 125 MHz carrier frequency, as asserted in the project scope (Section 1.2.1). The receiver exciter, frequency distribution unit, and timing distribution unit of NeXtRAD are briefly described as they connect directly to the transceiver and have some influence on its operation.

1.3.2 Implementation

The implementation of the digital transceiver system and tactics for meeting the user requirement are the focus of Chapter 3.

A set of application test procedures (ATPs) designed to meet the user requirements are developed Section 2.2.1. Each ATP consists of one or more experiments which test the digital transceiver's capabilities against the requirements. In Section 2.2.1 each user requirement is discussed and test procedure strategy developed with due consideration of the Cobalt's hardware constraints. A summary of the user requirements, their interpretation, and the ATPs developed to test them are summarized in Table 5.1.

The digital transceiver hardware is examined in more detail in Section 3.2. The board's signal processing resources consist of three 200 MHz A/D modules and a dual channel D/A chip. High performance digital signal processing IP cores come pre-installed on the FPGA. These digital signal processing cores are accessed by functions and structures in the ReadyFlow software C libraries –

there is no need to develop FPGA IP cores to accomplish the routine signal processing tasks, although the system can be reconfigured to do this with the optional GateFlow software package from Pentek. The manufacturer's software development philosophy for the Cobalt board is briefly explained, and the controller program versions written to meet the user requirements are elaborated on. It must be stressed that the task of writing software for the Cobalt module using the ReadyFlow board support package from Pentek is not trivial. Assistance from product specialists at Pentek was required to correctly set up the board for successful multichannel operation as per the user requirements, and this kind of support is routinely provided with many of Pentek's software defined radio systems.

Mathematical expressions for the transmitted and received waveforms are presented in Section 3.2.2. These make clear what expressions were used to generate the baseband linear frequency modulated (LFM) pulses. The standard pulse used in the system was a 50 MHz bandwidth LFM pulse with a $10\mu\text{s}$ length. Analytic expressions for the received and transmitted waveforms at the intermediate frequency help clarify the need to ensure phase coherent up- and down-conversion of signals between digital and analogue domains.

The transmit signal chain is scrutinized in Section 3.2.3, together with the frequency plan for upconverting the baseband samples from digital storage to the intermediate frequency. Some of the hurdles to achieving phase-coherent, low-jitter output are also discussed, in particular the need to synchronize the phase of the digital upconverter's numerically controlled oscillator on external trigger events is explained.

The module used to generate waveforms in the Cobalt is a Texas Instruments DAC5688 16-bit D/A converter. A block diagram is presented in Figure 3.4, which shows how complex samples from digital storage are interpolated, upconverted and output as an analogue signal at the 125 MHz IF. The frequency plan for effecting this is shown in Figure 3.5.

The receive signal chain and frequency down-conversion plan are presented in Section 3.2.4. Unlike the transmit chain, digitization and digital down-conversion are performed by different modules on the Cobalt board. Digitization is done by three ADS5485 16-bit analogue to digital converters, and the multi-channel digital down-conversion is implemented on pre-installed IP cores on the FPGA, one for each receive channel. The frequency plan for converting from the IF to complex baseband is shown in Figure 3.8. As with the transmit chain, it is important that the digital downconverter numerically controlled oscillators are reset on external trigger events to ensure phase coherency between pulses.

The typical equipment setup for measurements is shown in Figure 3.9. The items used to execute the ATPs included the following:

- the Cobalt XMC module and its host computer in an industrial enclosure,
- a signal generator to serve as the Frequency Distribution Unit (FDU),

- an arbitrary waveform generator to mimic the signals which would ultimately be provided by the Timing Control Unit (TCU),
- an intermediate frequency signal splitter, used to generate three identical signals from a single input when testing multi-channel digitization,
- several lengths of CNT100 coaxial cable to route intermediate frequency signals between D/A, A/D modules and measuring instruments,
- spectrum analyzers and oscilloscopes to measure frequencies, spectra and waveforms.

A low-power prototype of the active node of the radar was constructed from available equipment, as described in Section 3.3. Measurements taken from the roof of the George Menzis building on the University of Cape Town’s upper campus were used to give confirmation that the digital transceiver satisfied basic signal processing requirements. The equipment used for this prototype included:

- all the equipment used to test the system against the user requirements,
- the REX,
- low-loss RF cables to connect the REX to RF amplifiers,
- various antenna systems for L- and X-band tests.

The different configurations, three for L-band and one for X-band, are summarized in Table 3.3.

1.3.3 Acceptance Testing

The acceptance test results are given in Chapter 4. Waveform generation was tested in Experiment A. Phase-stable, low-jitter output of sine waves and the LFM pulse at the 125 MHz IF was possible using the final version of the controller program, satisfying the user requirements for signal generation. An example pulse is shown in Figure 1.2.

Experiment B (Section 4.2) was focused on multi-channel digitization of waveforms at the intermediate frequency. Loop-back measurements verified that the digital downconverter IP cores were working as expected for sine waves. In addition, the DDC numerically controlled oscillators were configured to reset phase to zero on the external trigger. Polarimetric X-band measurements would be impractical without this reset because an unknown and unpredictable phase difference between the vertical and horizontal channels would be introduced at each trigger event.

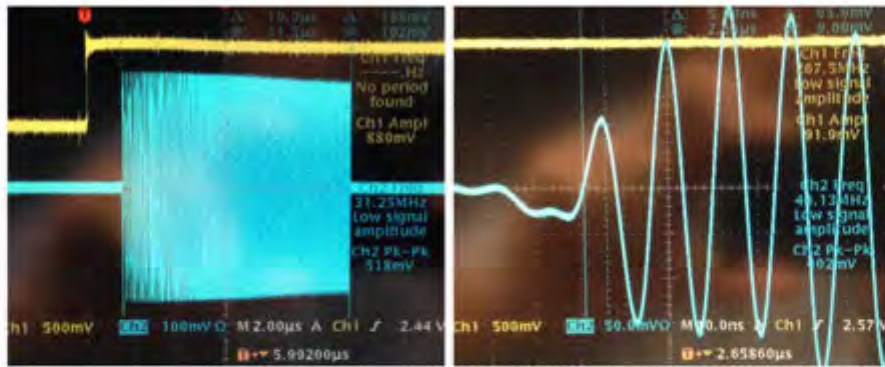


Figure 1.2: Phase-stable, low-jitter DAC output showing a 50 MHz LFM pulse on a 125 MHz carrier frequency. This trace shows how consistently the DAC output waveform (blue) is generated with respect to the rising edge of the trigger signal (yellow).

The impulse response (autocorrelation of the LFM pulse) and the overall system jitter were tested in Experiment C (Section 4.3). To test the up- and down-conversion frequency plans together, Experiment C.i. involved doing a loop-back measurement using the full-bandwidth LFM chirp. The recorded pulse was used to calculate the compressed response of this waveform. Comparing it with the $S_a(t)$ approximation for large time bandwidth product pulse compression showed that the system was producing results consistent with theory, as can be seen in Figure 1.3. Loop-back measurements of the RF signal were also calculated and produced similar results, although some widening of the time width was expected and observed.

The Experiment C.i. was designed to test the jitter of the system. This was done by generating a sine wave using the full upconversion chain of the transmitter, and then downconverting this signal to a constant phase value using the DDC cores on each receive channel. Each DDC core was tuned to exactly the DAC output frequency to achieve this. Any variation in transmitter output delay or phase would manifest as changes in the phase of the downconverted signal. The test showed that there was uncertainty in the output delay of the signal from the DAC, but only between separate measurements. During a single measurement, however, phase remained constant and jitter was measured to be less than 280 ps. This consistency within a single measurement presented no obstacle to doppler processing of the recorded data post-experiment. The user requirement for phase stability and low jitter were therefore satisfied.

Experiment D (Section 4.4) concerned the control of generation and acquisition of waveforms. These processes are controlled by means of linked lists in the controller program source code. The variables controlling the operation of the transmit and receive chains are defined and their function explained. An example of waveform acquisition is shown in Figure 4.23 on page 71, showing the first few pulses in a recording.

Experiment E was conducted to determine the maximum pulse repetition frequency of the digital transceiver. It was tested on two different (but quite similar) host computer systems, one at Pentek

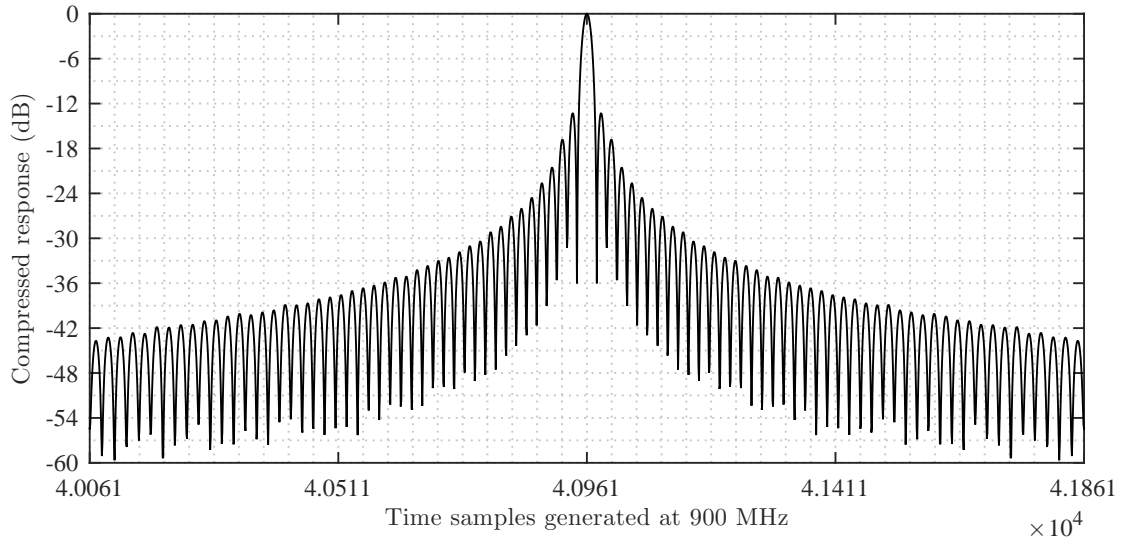


Figure 1.3: Normalized compressed response of the 50 MHz LFM pulse, showing the characteristic $Sa(t)$ form at the peak output. The 900 MHz sample rate is achieved by zero-padding of the recorded data blocks – the actual raw samples from the ADC are written to disk at one-tenth this frequency.

in the USA, and the other at UCT. It was determined that the Cobalt module and the host computer would be able to operate at and higher than the required 2 kHz PRF, whilst digitizing signals from three ADC channels. This exceeded the original user requirement which called for simultaneous digitization of two channels at most.

To confirm the operation of the digital transceiver apart from the application test procedures, the prototype system was built and used to take measurements from the vantage point of the George Menzies building rooftop with four different experimental configurations. The site of many similar measurements, the rooftop offered several nearby targets for test measurements, both stationary and moving. To start with, the nearby PD Hahn building was targeted for measurements. Pulse compressed monopulse recordings showed peaks in the graph corresponding to this large target and several other likely scatterers in the line of sight. With phase coherent measurements taken at 1 kHz, it was also possible to detect moving cars and pedestrians on nearby roads by their doppler shifts. Throughout these tests measurement parameters were interpreted from a text file parsed by the Cobalt controller program as they would be in the completed radar system, satisfying the final user requirement.

1.3.4 Conclusion

The Cobalt system was successfully configured for use as multi-channel pulse-doppler transceiver for NeXtRAD. The frequency plan to generate and digitize the IF waveforms compatible with REX was tested by loop-back measurements and checked by comparing the pulse compressed response with the theoretical expectation. The measurements of the phase and jitter variation in Experiment C.ii.

showed that the system was stable with very low jitter on the transmit and receive chains, satisfying the user requirements for overall system jitter phase stability. Transmit and acquisition control was effected by means of the linked list controllers in the Cobalt module and proven operational. As a final demonstration of the Cobalt's suitability, several low-power radar measurements successfully detected both static and moving targets. Overall, there is a reasonable expectation that the digital transceiver will be suitable for use in the active node. With minor changes the Cobalt module can function in receive-only mode in the passive nodes of the final multistatic system.

Chapter 2

System Overview

This chapter provides the background material needed to understand the operation of NeXtRAD's digital transceiver. Specifications of the various subsystems are briefly presented to give context for the digital transceiver. Subsystems which interface directly with the Cobalt, i.e. the REX, TCU and FDU are described in more detail.

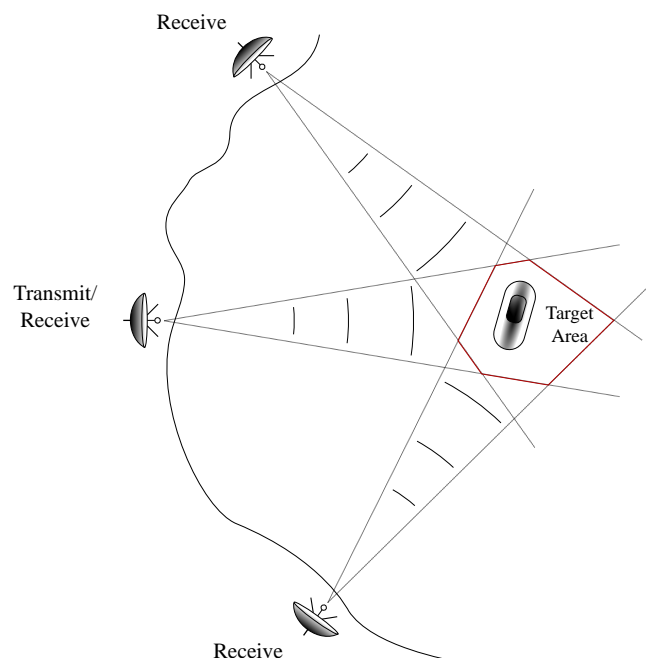


Figure 2.1: One example of multistatic radar topology, showing three nodes on a coastline cooperatively focused on a single target. NeXtRAD's configuration employs a single active node and two passive nodes, target range from about 2-10 km. This project is concerned with the digital transceiver unit in the active node only.

2.1 NeXtRAD's Principle of Operation and System Specifications

NeXtRAD is a multi-static, dual-band, polarimetric radar system intended for ocean surveillance. The development of NeXtRAD as a follow-on from NetRAD has been detailed by Inggs et al [5]. It is comprised of three nodes distributed along a coastline, as illustrated in Figure 2.1. There is a single active node (Node 0) illuminates the target area with the radar beam. The beam has an azimuth beamwidth of 10° , and a maximum range of 10 km. The other two receive-only nodes have the same antenna beamwidth and are focused cooperatively on the same area by motorized pedestals.

Pulses transmitted by the active node are reflected by the radar scene and are detected by all three nodes. GPS-disciplined oscillators in each node make it possible to accurately determine the time of flight of a pulse along trajectories from Node 0 to any node. With some calculation it is possible to accurately determine the location of a target from the echoes recorded by any two of the nodes.

NeXtRAD incorporates a motorized pedestal system to aim the antennas at a common target area for each experiment. The lack of automated pedestals was a major drawback for NetRAD. Also incorporated are high definition video cameras which will record the view of the target. This provides a visual reference of the sea state and antenna orientation which is useful after measurements have been taken. GPS coordinates are used to determine the steering angle for each antenna. Each node is capable of recording in either V or H polarization in L-band, polarimetrically in X-band. This allows for six modes of operation; four modes in L-band, two in X-band operation. The NeXtRAD specifications are given in Table 2.1.

In a typical experiment, the radar will transmit at a 1 kHz PRF for 180 s. Recorded data are stored in a single binary file for each recording channel. After measurements, data files are transferred from the digital transceiver host PC to a command and control computer via a wireless network which links all nodes. Video footage of the target area is also captured by cameras mounted on the transmit pedestal at each node. These recordings provide a visual reference for checking that the antennas are aimed at the right target and are also useful for recording the sea state.

Table 2.1: System Specifications and Parameters

Radar Parameters		
Frequency	L-Band	X-Band
Tx Center Frequency	1.3 GHz	8.35 GHz
Tx Power: Low Power Prototype	< 24 dBm	< 24 dBm
Tx Power: Full Amplification	1.4 kW	0.4 kW
Pulse Length (Typical)	10 μ s	10 μ s
Pulse Type	LFM Chirp	LFM Chirp
Pulse Bandwidth	50 MHz	50 MHz
Pulse repetition frequency	1 kHz - 2 kHz	1 kHz - 2 kHz
Antenna Parameters		
Frequency	L-Band	X-Band
Antenna Type	Reflector Dish	Conical Horn
Polarization	Dual	Dual
3 dB Beamwidth	10°	10°
Center Frequency	1.3 GHz	8.35 GHz
Operating Specifications		
Range Resolution (Rayleigh)	3 m	
Azimuth Resolution – Monostatic	10°	
Azimuth Resolution – Bistatic	Geometry dependent	
Azimuth Resolution – Multistatic	Geometry dependent	

2.2 System Hardware Considerations and the Digital Transceiver

The single active node and one of the passive nodes of the system are shown in Figure 2.2. Node 0 is responsible for generating and recording pulses, whilst Nodes 1 and 2 are receive only.

The active node's role can be summarized as follows: *To generate and transmit radar pulses from storage and to receive and digitize the reflections from the target scene.* Passive nodes are identical to the active node, except that they do not generate pulses. Components that make up the active node include:

- a command and control laptop computer which manages all experiments,
- an industrial computer which hosts the Cobalt transceiver module,
- the Receiver Exciter (REX),
- the Timing Control Unit (TCU),
- the Frequency Distribution Unit (FDU),
- RF frontend comprised of many subsystems, including the X- and L-band antennas,
- motorized pedestals which point the antennas,
- a hardware enclosure and power supply systems, etc.

A simplified system block diagram of the active node components listed above is shown in Figure 2.3. The digital transceiver, or Cobalt module, in this diagram is the primary focus of this report.

2.2.1 User Requirement - Digital Transceiver Module

The system engineer, Professor M. Inggs set the following user requirements for the digital transceiver (DT) [6]:

- 1 The DT shall generate the 50 MHz bandwidth LFM chirp signal at the 125 MHz intermediate frequency (IF) from a preloaded waveform on each LVTTTL hardware trigger received. The output signal level 3 to 7 dBm.
- 2 Output sample rate shall be around 800 MHz at 16-bit resolution.
- 3 Generated waveforms shall be transmitted with fixed phase relative to the external trigger event, i.e. successive pulses shall be identical.

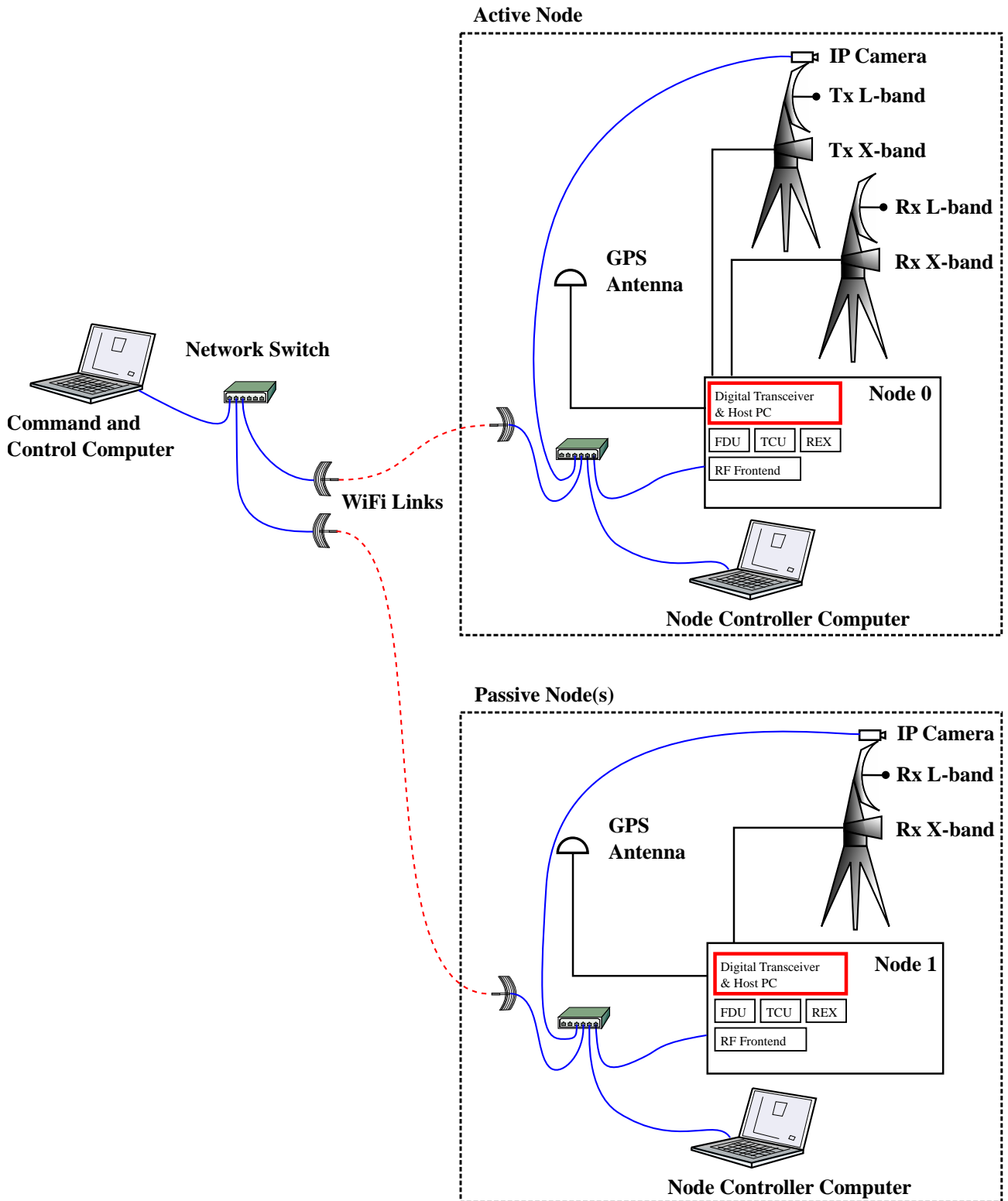


Figure 2.2: The NeXtRAD system in bistatic configuration with the active and passive node shown. In multistatic configurations there are two passive nodes present. The digital transceiver in each node is bordered in red. The active node digital transceiver is of primary concern in this project, and it serves as the template for passive nodes as well.

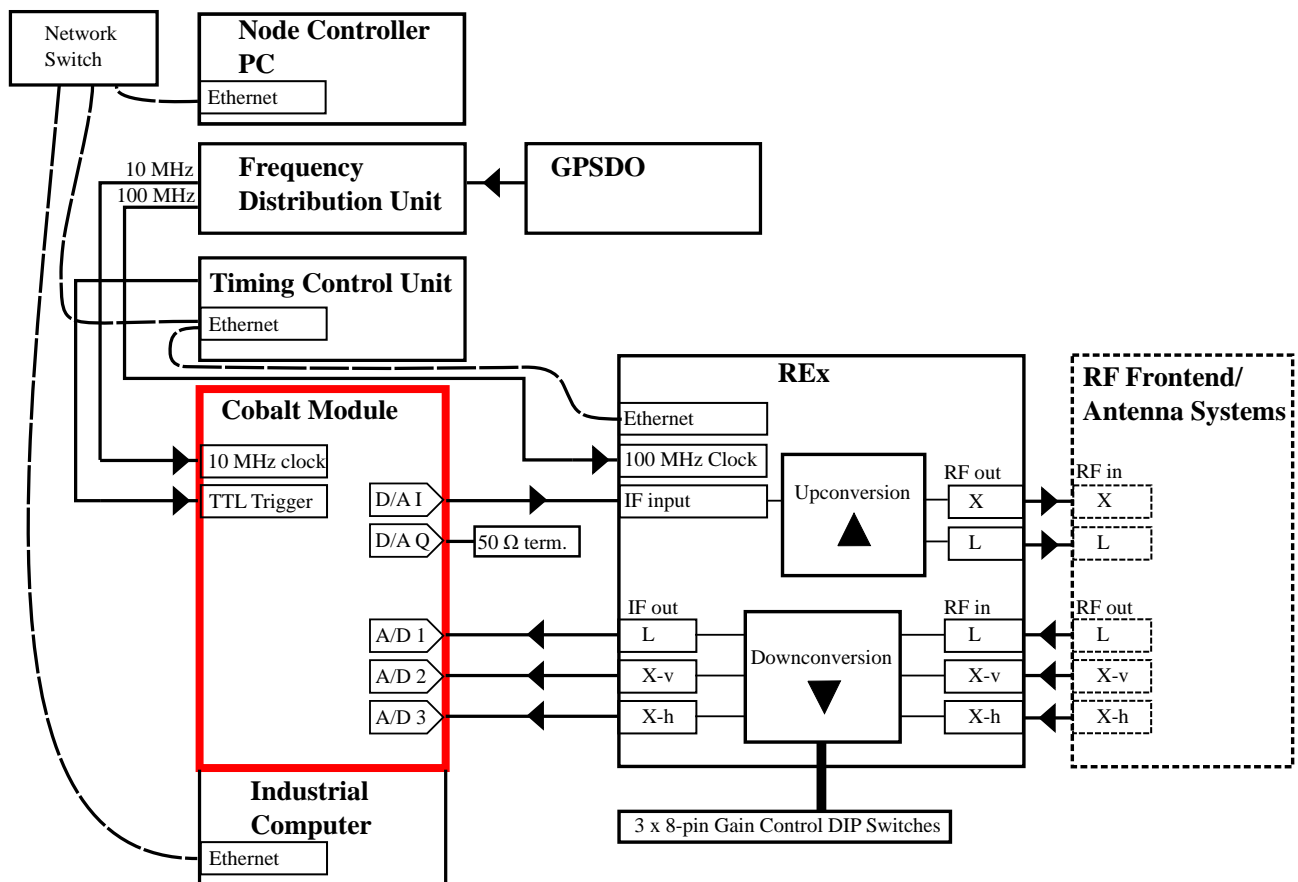


Figure 2.3: A simplified system block diagram of the NeXtRAD active node and its subsystems. The digital transceiver module, bordered in red, is hosted by an industrial computer which interfaces with the Node Controller PC via Ethernet. The accepts a TTL trigger signal from the Timing Control Unit and a 10 MHz reference from the Frequency Distribution unit. The Cobalt delivers one transmit signal to REX and accepts three from it, all at the intermediate frequency of 125 MHz.

- 4 The DT shall digitize and downconvert to complex baseband the input signal on all three ADC channels simultaneously in response to a hardware trigger, with predictable phase on consecutive events. Data shall be recorded to disk as one file per channel.
- 5 ADC digitization frequency shall be around 200 MHz, at 16-bit resolution.
- 6 The DT shall not contribute more than 500 ps of jitter to the system.
- 7 The DT shall synchronize internal oscillators to an external, phase-stable, 10 MHz reference clock.
- 8 The delay of transmit and recording after the trigger event shall be independently adjustable.
- 9 The transceiver shall have the capacity to generate and digitize 180 000 pulses in a continuous recording, with 8 192 complex samples per pulse.

- 10 The DT shall have the capacity to generate/digitize waveforms at a minimum PRF of 2 kHz in response to a supplied 3.3V LVTTTL external trigger.
- 11 No pulse shall be transmitted on the first trigger, this facilitates measurement of noise and environment signals only.
- 12 The DT and host computer shall accept predetermined experiment parameters in the form of text file detailing measurement requirements. Parameters shall include (at minimum) the number of pulses to generate/digitize and the waveform to transmit.

2.2.2 Other Subsystems

The other subsystems and components of the active node are summarized here.

The Receiver Exciter. This receiver exciter subsystem was manufactured by Reutech Radar Systems [2, 7, 8] and it interfaces most directly with the digital transceiver. As such it is important that the Cobalt is able to supply the signals to and receive signals from the REX at correct power levels and frequencies.

RF Front End. Developed by Stevens [9], this system amplifies the RF signals from the REX for transmission and also amplifies the received echo signals. Transmission in both X- or L-band is possible in either vertical or horizontal polarization. However, rapid switching between polarizations on transmit is precluded by the lack of a high powered RF switch at either band. Thus the transmit polarization is selected pre-experiment by connecting the high power RF cables to the appropriate terminal on the antenna feeds.

Antennas. The polarimetric X- and L-band antennas were designed by Mr Cheng and Mr Paine respectively [10, 11]. The antennas had a 10° azimuth beamwidth in both polarizations. X- and L-band antennas are attached to the same pedestal. One of the antennas is used transmitting and the other for receiving. These and other antenna systems were used in low power demonstrations of the system, documented in Chapter 4.

Timing Control Unit. The TCU is responsible for supplying highly accurate timing signals to the high-powered amplifiers in the RF frontend, REX, and the digital transceiver. The TCU is based on the UCT-developed Rhino board, which uses a Spartan 6 Xilinx FPGA. Using an FPGA enables the TCU meet the stringent requirements for timing accuracy, which is important when generating the PRF trigger. FPGAs implement digital logic directly, which allows their output signals to be controlled to within a few nanoseconds. Microcontrollers without real-time operating systems do achieve this level of timing accuracy. The BORPH operating system was used to implement the timing core on the FPGA by Burger [3]. The TCU generates the PRF trigger signal which initiates both pulse generation and recording in the digital transceiver. The TCU also sends frequency-selection signals

to the REX. The high-powered X- and L-band amplifiers in the RF front end are also switched by the TCU. In testing and development work in this project, the TCU signals were mimicked by an arbitrary waveform generator.

Frequency Distribution Unit and GPSDO. Each node has its own GPS disciplined oscillator unit (GPSDO), which generates a highly stable 100 MHz clock signal, on which the REX is dependent. The frequency distribution unit uses this frequency as a reference for generating 10 and 100 MHz clock signals required by the digital transceiver and the REX in the active node. It also provides a highly precise pulse per second used to synchronize transmission and acquisition of signals across nodes. In this project, the phase-stable 10 MHz reference frequency was supplied by a laboratory signal generator.

Pedestals. Sky-Watcher AZ-EQ6 GT telescope tripods and mounts were adapted for use with NeXtRAD's antenna systems. These mounts were motorized and could be automatically steered to point telescopes, or in this case antennas, in any direction. This was accomplished by means of a pedestal controller which was programmed by the controller computer of each node. All pedestals cooperatively focus antennas on a common target area during measurements.

Enclosures. These containers provided ingress protection for the radar's sensitive electronic equipment from moisture ingress in coastal regions.

Power Supply. Each node can be powered by a standard 220 VAC source from a mains supply. Where this is unavailable a generator and battery backup system provide power.

2.3 Summary

This chapter provided a high level review of NeXtRAD, laying the groundwork for operation of the digital transceiver. Each node of this multistatic system will employ a Cobalt XMC module to do transmission/digitization of radar signals at the intermediate frequency. In the transmitting node this module will interface directly with the REX, TCU and FDU as shown in Figure 2.3. Configuring these three systems was beyond the scope of this project. However, it was necessary to ensure that the Cobalt module could interface directly with them. A laboratory signal generator would be used to supply a stable 10 MHz reference clock to both the digital transceiver and to an arbitrary waveform generator (AWG), which the FDU supplies in the final system. The AWG served as a TCU during testing, generating LVTTTL compatible trigger pulses which drove the digital transceiver.

The user requirements for the digital transceiver were listed in Section 2.2.1. These requirements provided direction for development of the Cobalt controller code. The user requirement sets the standard for waveform generation and digitization, and defines the means by which the Cobalt will receive instructions from the command and control PC. The user requirements will be interpreted to formulate the Application Test Procedures in the next chapter.

Chapter 3

Implementation

To meet the user requirement, an application test procedure (ATP) is presented in this chapter. The ATP is a set of experiments designed to evaluate the conformance of the digital transceiver system with the user requirements presented in Section 2.2.1. There is some freedom of interpretation with these, and the tests derived are intended to verify the DT's conformance by multiple measurements.

This chapter includes a more complete description of the DT system. The Pentek Model 71621 Cobalt digital transceiver module was procured to meet the user requirements. Use of the Cobalt Model 71621 board and its associated ReadyFlow software are explained. The software development philosophy of the ReadyFlow package is somewhat arcane, hence the introduction will be of benefit to future developers working with the Cobalt. To successfully program the Cobalt board requires a good knowledge of both the digital signal processing hardware and its limitations, as well as familiarity with the ReadyFlow software. The design approach taken to develop the Cobalt controller program as a pulse-doppler radar transceiver using these tools is presented in this chapter.

A key consideration for the DT is frequency planning for both the transmit and receive signal paths. The signal processing hardware in the Cobalt will dictate the sample rate and bandwidth of signals that can be generated, and how the incoming IF signals will be digitized and then stored. The transmit and receive signal chains are explained and justifications are presented for the choice of ADC and DAC sample rates, digital up and downconverter tuning frequencies, and interpolation/decimation rates.

As part of the development of the DT, but unrelated to any specific user requirement, was the integration of a low-power prototype radar. These prototypes were built using RF components from the microwave and radar laboratories, the dual-band REX, and a variety of antennas. There were four different configurations used to test the DT. Each measurement proved extremely helpful in identifying problems in the setup of the digital transceiver. Single pulse measurements taken from the George Menzis building roof showed that large buildings nearby were detected at the expected ranges. Range

doppler plots obtained from X- and L-band measurements with a properly configured DT were successful in detecting moving and static targets.

3.1 User Requirement Interpretation and Application Test Procedure Derivation

The ATP presented in this Chapter is essentially a set of experiments designed to test the DT against user requirements in Section 2.2.1 on page 14, which are reviewed here. The interpretation and experiment design for testing each of these often requires several related tests, performed in succession. The strategy used is to test each capability by increments, until the total user requirement is met.

User requirement 1 is for a basic transmit pulse; the DT needs to generate a 50 MHz bandwidth LFM pulse on a 125 MHz carrier. The frequency plan developed for this is detailed in Section 3.2.3. Getting the waveform to generate on an external trigger event is fairly trivial. Developing a test procedure requires knowledge of the signal processing chain in the Cobalt module. Similarly, the high 800 MHz output rate of requirement 2 will depend on the interpolation factor and the rate at which data are read from memory on the Cobalt board. Lower output frequencies are possible at the cost of slightly reduced spectral purity.

Requirement 3 demands phase coherence between successive pulses, which is necessary for pulse-doppler processing. Because of the data input rate limit of 250 MHz on the DAC module, the digital upconverter (DUC) and interpolation must be engaged to reach the 125 MHz IF whilst operating at the high output frequency of requirement 2. The upconverter is essentially a multiplier which generates the product of the complex waveform and sinusoid before interpolation filters increase the output frequency of the DAC. The DUC does introduce phase shift to the output waveform which must be controlled to ensure identical output pulses. A related problem is the variation in the DAC output delay after the trigger event. Both phase and time output jitter can have a detrimental effect on post-processing and both must be minimized. Both can be measured using an oscilloscope with acquisition triggered by the external trigger signal supplied to the DT. The output frequency and DUC tuning frequency can be reduced to below 100 MHz (lower frequencies are easier to measure) and the phase and output jitter eliminated. Once a sine wave can be successfully transmitted with stable phase and low transmit jitter, the full LFM waveform can be generated at higher DAC output frequencies and interpolation rates.

It must be emphasized here that in the digital transceiver (the Cobalt module) the NCO used in the up-conversion path operates at a frequency different from the NCO frequency used in the down-conversion path. This is different from the situation in the REX, which only does analogue processing and uses the coherent local oscillator frequencies for multipliers in its transmit and receive chains. Thus in

REX any phase introduced to the transmitted signal by the analogue mixer in the up-conversion chain is removed by mixing in the down-conversion chain. This is not the case with the digital transceiver. Although both the DUC and DDC NCO frequencies are derived from a common 10 MHz source, the phase difference between them at the start of each PRI may not be consistent between pulses. This will produce a phase shift in the pulses reflected from a stationary scatterer which have nothing to do with the scatterer's dynamics. There are at least two ways of avoiding this.

The first would be to allow the NCOs to run freely and ensure that trigger events occur only when the phase difference between the DUC and DDC NCOs is at a fixed value. To use an external trigger to accomplish this would be awkward because this signal would need to arrive exactly when the phases of the NCOs are at a fixed difference. If the trigger were internally generated, perhaps by the DAC linked-list output control engine on the FPGA, ensuring constant phase difference would be fairly straightforward if the timing of each transmission was correctly set. ADC acquisition could be initiated by a synchronization signal generated in the DAC output control engine. However, this would make the digital transceiver the trigger source for each node in the multistatic radar, which would complicate the system because this is in fact the role of the timing control unit.

The alternative approach was to reset the phase of the digital numerically controlled oscillators to a known value at the arrival of the external trigger event. This would ensure that the phase of the transmitted IF pulse would be precisely the same, i.e. the output waveform of the DAC in-phase (or quadrature) channel plotted on an oscilloscope would be identical (ignoring noise and a tiny amount of clock jitter) no matter when the external trigger event occurs. The same applies to the ADC channels, which will digitize the transmit pulses of the DAC with complete consistency because the DDC NCOs are reset by the same trigger signal. This configuration keeps things simple because the PRF is entirely determined by the timing control unit and any phase introduced by up- and down-conversion chains are constant between pulses and therefore irrelevant.

As with 1 to 3, requirements 4 and 5 demand an understanding of the hardware in the receiver signal processing chain of the DT. A more in-depth examination of the down-conversion chain in the Cobalt module is offered in Section 3.2.4, together with a frequency plan for digitization and down-conversion to complex baseband. The maximum sampling frequency of the ADCs on the Cobalt board is 200 MHz, consequently the 125 MHz IF signal is in the second Nyquist zone and therefore undersampled. This has an impact on the DAC frequency as all sample clocks are derived from a common voltage controlled crystal oscillator. Digital down-converters (DDC) that translate sampled waveforms to complex baseband also use digital multipliers similar to the DUC. These also introduce phase shift to digitized waveforms. Testing the digitization and frequency was done by supplying a sinusoid to the ADCs with the DDCs active and plotting the stored waveforms to verify that they were of the expected frequency.

To test synchronization of multiple DDC channels on the Cobalt, the procedure was to drive all three ADC channels with an identical sine wave. This triple-sine wave was obtained from a splitter driven

by a signal generator. Digitization would then occur on each trigger event which would generate near identical (ignoring noise) waveforms for all channels – easily verified by plotting the raw data samples. This would satisfy requirement 4 for phase coherency on digitization.

A reliable way of testing the DT against requirements 1 through 5 was to do the following two tests:

1. A loop-back recording of a sine wave to DC, employing both the up and down-conversion chains and their associated NCOs.
2. Store a loop-back recording of the 50 MHz LFM pulse, then calculate the autocorrelation function and compare it with theoretical predictions.

The first test would show that the system was capable of generating and digitizing a waveform without introducing phase drift. If phase drift were present, it would manifest as gradual oscillation in the downconverted signal. If not, the phase of complex samples from the DDC would remain constant. In addition, this test would partially fulfill requirement 6 for low overall system jitter, although this would really be a measurement of the relative jitter between the DUC and DDC chains, not absolute jitter of the system relative to a perfectly natural clock.

The second test would show that whole frequency plan was working as expected. The autocorrelation of the transmitted and received pulses would theoretically produce sine-over-argument function in the time domain. Errors in the frequency plan or waveform generated would appear as deviations from the theoretical autocorrelation of an LFM waveform.

Requirement 6 for low system timing jitter depends on the phase stability of the 10 MHz reference signal dictated by requirement 7. Jitter in the reference clock would be conveyed to DAC and ADC clocks as well. Without a perfectly stable reference clock driving ideal ADC and DAC chips to compare with the physical components it was not possible to determine exactly how much jitter the DT contributed to the system. However, it was possible to measure with an oscilloscope (to within 200 ps) how much jitter was present in the DAC output waveform. Any variation in the delay between arrival of the external trigger and the output waveform would manifest as integer multiples of the DAC clock period T_{DAC} . In experiment A the output clock frequency was set to 200 MHz, giving a clock period of 5 ns. With a time resolution of 0.2 ns, any output jitter due to DAC clock could be readily seen on the oscilloscope.

Requirements 8 through 11, which related to control of the digitization and generation processes in the Cobalt, were expected to be within the capabilities of the module. Timing of generation and digitization of waveforms is controlled by means of linked list engines, which determine the number of samples to transmit/digitize, delays after trigger events, number data transfers (i.e. pulses) to process, etc. The exception is requirement 10, because the maximum PRF at which the DT can operate reliably depends on how much data is stored per pulse, the memory access times of the host

system, the amount of other tasks the operating system is burdened with, and many other factors. Maximum data rates are constrained by the Cobalt host computer's memory read and write latencies. An indication of the maximum PRF can be obtained by testing the DT with successively higher PRFs until failure occurs.

Requirement 12 is for DT to accept measurement parameters from a remote user in the form of a text file. The text file is distributed from the master controller computer via the network to each node. The file is then parsed by the DT controller program and used at each initialization. These capabilities were added to the controller program during development as required, and once incorporated, used for subsequent experiments.

A summary of the proposed Application Test Procedures are listed in Table 5.1, which is not a complete listing of the measurements done to verify each capability of the DT. Additional tests are detailed in Chapter 4.

3.2 Overview of the Digital Transceiver

The Pentek model 71621 "Cobalt" model was procured to work as the transceiver in the NeXtRAD system. The Cobalt provides a complete software defined radio interface which is intended for use in radar applications. The Cobalt board incorporates the following significant capabilities:

- 800 MHz, 16-bit D/A module with complex I/Q output, integrated 8x interpolation filter and digital upconverter.
- Three 200 MHz, 16-bit A/D modules.
- Virtex-6 LX240T FPGA installed with digital upconverter and downconverter IP cores.

An external reference clock can be used to synchronize sample clocks of the D/A and A/D chips, and the board accepts external triggering via a front panel synchronization bus. The board is programmed in C. Board resources are initialized and accessed by callable C functions included in the ReadyFlow Board Support Package (BSP). The ReadyFlow package produced by Pentek is used to program many of their products. The library includes data structures, board and register level routines to configure every resource on the Cobalt. High performance DSP cores come pre-loaded on the LX240T FPGA. IP cores include three digital downconverter cores with decimation filters. Reconfiguring the FPGA requires additional software from Pentek and was unnecessary for this project. 1 GB of DDR3 on-board memory is used to store waveforms transmit and to buffer recorded data from the DDC channels before it is written to system memory via the PCIe interface.

Table 3.1: Summary of User Requirements (UR) for the digital transceiver and the associated Application Test Procedures

UR	Interpretation	Experiment(s)
1-3	Generate 50 MHz LFM waveform at IF, stable phase, low jitter. Validate upconversion frequency plan.	(A.) Enable the DUC and measure DAC output with oscilloscope for phase consistency and output jitter. Measure output waveform spectrum using a spectrum analyzer to ensure that 50 MHz 6 dB spectrum width is achieved on the 125 MHz IF.
4-5	Digitize sine waves using the DDC, ensure equal phase for each NCO. Validate the down-conversion frequency plan.	(B.i.) Digitize a waveform from a signal generator, ensure that the digital downconverters are operating correctly by inspection of raw data. (B.ii.) Ensure that all three DDC channels are synchronizing by digitizing an identical sine wave from a split signal generator output.
1-5, 6-7	Simultaneous triggering of transmit and digitization processes with low system jitter.	(C.i.) Calculate the autocorrelation output (matched filter output) of the 50 MHz bandwidth LFM chirp at the 125 MHz IF. Compare against theoretical $Sa(t)$ output*. (C.ii.) Loop-back measurement: Generate a sine wave using the DUC and digitize in all three channels with the DDCs tuned to exactly the generated frequency. A constant-phase complex value should result.
8, 9, 11	Control acquisition and transmit of waveforms, fine adjustment of delay after triggering for these processes.	(D.) Configure the linked list control engines for acquisition and transmit chains. Examine loop-back recording raw data to ensure that the acquisition is working as required.
10	Operate at PRF exceeding 2 kHz with multichannel acquisition	(E.) Test system to failure: Conduct successive loop-back tests at increasing PRFs until the program becomes unstable (i.e. crashes), or fails to digitize/transmit correctly.
12	Accept measurement parameters from a text file	(F.) Incorporate a parser into C source code for the DT controller program and use as part of all tests.

* The sine over argument function: $Sa(t) = \frac{\sin(t)}{t}$

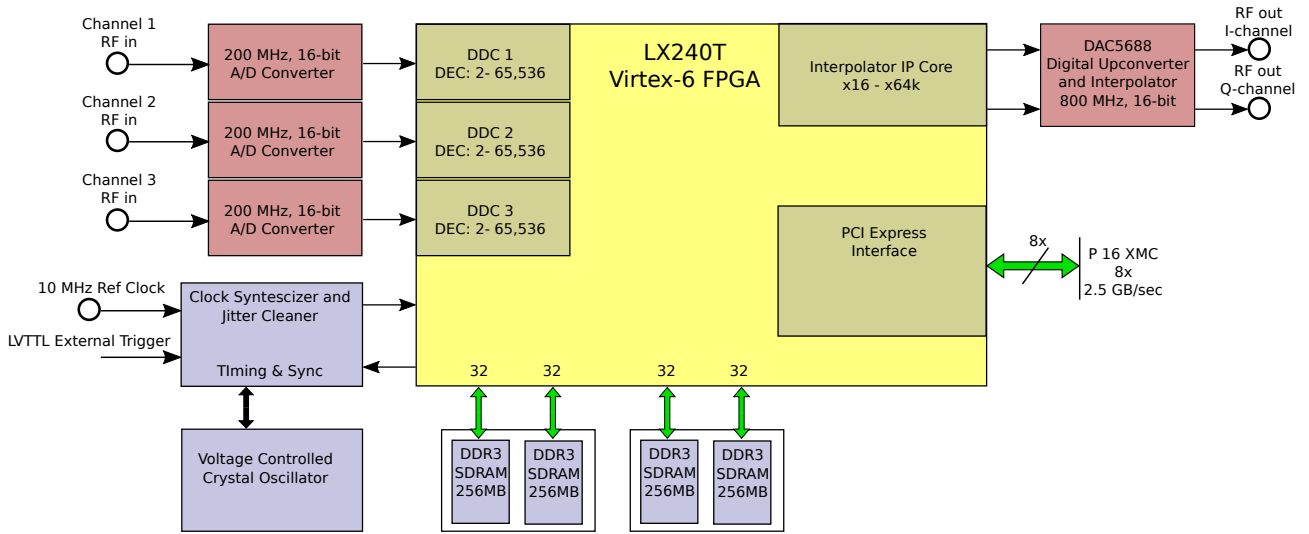


Figure 3.1: The Pentek Model 71621 Cobalt transceiver block diagram, showing the three A/D modules and dual output channel D/A unit, as depicted in the operating manual [12]. The DAC5688 incorporates interpolation filters and digital upconverter to translate low data rate (< 250 MSPS) waveforms to significantly higher output frequencies of up to 800 MHz. The A/D units sample at 200 MHz (max) and stream data directly to DSP IP cores on the LX240T FPGA. The digital down-converters IP cores incorporate decimation filters and complex multipliers which generate I and Q channel samples. 1 GB of DDR3 RAM is available for storing transmit waveforms. A direct memory access engine on the FPGA uses the PCIe interface to transport data from the DDC core trio directly to system memory.

An image of the Cobalt board is shown in Figure 3.2. The board is housed in a Hartmann industrial computer chassis with CompactPCI backplanes. Also enclosed is an Allegero PC, which is equipped with an Intel i7 CPU with 8 GB of DDR3 RAM and a 120 GB solid state hard drive. The Allegero is used to program the Cobalt module.

3.2.1 Controller Program Development

The task of configuring a Cobalt module for several signal processing operations is not straightforward. Programming the board combines hardware and software development. To successfully program the board for a signal processing task requires that developers have an understanding of hardware limitations combined with thorough knowledge of tools available in the ReadyFlow libraries. ReadyFlow provides direct access to configuration registers for the A/D and D/A chips, clock synthesizer and VCXO, DSP IP cores on the FPGA, and many other modules. Although the software does simplify board setup by automatically configuring some modules, such as the clock synthesizer and VCXO, to a usable default modes, it will not prepare the board for custom signal processing tasks. Data paths, sample rates, interpolation/decimation factors, triggering, and other digital signal processing considerations all need to be set up by the programmer in fairly sophisticated low-level C code. To aid with the development process, a set of example programs were included with



Figure 3.2: The Pentek 71621 -“Cobalt” transceiver. Image reference: Pentek 71620 documentation. The SSMC connectors for the reference clock, the dual DAC outputs, and three ADC input channels are visible on the right.

ReadyFlow to demonstrate some of the board’s capabilities. Examples demonstrate either waveform generation or digitization, but none of them show simultaneous transmit and digitization capability. At the time of writing, Pentek did not provide a ready-to-run pulse-doppler radar controller program for the Cobalt module. This would require simultaneous triggering of transmit and digitization on the board, although it is possible to develop a MIMO radar using several Cobalt modules running on a synchronization bus. This would allow each board to function either as a dedicated transmitter or receiver, and such configurations are not uncommon. Given the significant cost of a single module, using two different boards for transmit and receive was not an option. For NeXtRAD’s requirements, a program had to be written from scratch or developed from adaptations of supplied examples. Either approach would involve substantial work to meet the user requirements in Table 5.1. Details of the capabilities of three different programs, each of which were developed with the aim of meeting some or all the user requirements, are given in Table 3.2. The development trajectory of the final controller program is elaborated on in the following paragraphs.

First Controller Program

The first controller program, `baseline_doppler_demo`, was a very basic single channel pulse-doppler application program which operated at an IF of below 100 MHz. This source file was developed by an application engineer for an earlier customer. Using this program it was possible to generate 50 MHz bandwidth chirps at low carrier frequencies (with external triggering) whilst meeting the Nyquist requirement, but the sample frequency on both the A/D and D/A modules was limited to 200 MHz. The maximum data input rate of the D/A module was 250 MSPS, which restricted the frequency of a digitally stored waveform to 125 MHz. This was further reduced to 100 MHz because of a 200 MHz D/A sample rate. With some configuration changes to the board clock synthesizer, it was possible to run the DAC at double the ADC frequency whilst keeping the data rate equal to the ADC frequency. The data input rate to the DAC was kept at about 100 MHz, well below the 250 MSPS limit, and the interpolator increased the output sample rate. Using the upconverter in this way it was

possible to measure the output of the DAC on a spectrum analyzer. A frequency plan used to transmit these waveforms is presented in Section 3.2.3. Digitization of the 125 MHz IF would require undersampling as explained in Section 3.2.4. Lower frequency loop-back measurements were done which showed that the system was capable of generating sine waves in the 100 - 150 MHz bandwidth compatible with REX, but the transmitting the full 50 MHz chirp at the IF was problematic.

On the receive chain, the digitized samples were real-valued as the digital downconverter (DDC) for the input channel was not enabled, so generating I and Q channels would need to be done in post-processing. The clock synthesizer was not configured to accept an external 10 MHz reference clock. A second attempt was needed which would meet the requirement for an external reference and simultaneous operation of the DUC and DDC modules.

Second Controller Program

To improve on the first controller program, a new version called `baseline_uct_demo.c` was developed, an abbreviated code listing is given in Appendix A. This program enabled the DUC on the DAC5688 D/A module, and the DDC IP core. Configuring the clock synthesizer to drive the D/A and A/D sample rates of 360 and 180 MHz respectively made it possible to match the frequency plans developed in Sections 3.2.3 and 3.2.4. The major drawback of this program was that the numerically controlled oscillators (NCOs) in the DUC and DDC were not synchronized by the external trigger event. This resulted in effectively random phase of the output waveform from the D/A module. On the digitization side random phase was introduced to the recorded waveform by the downconverter (see Chapter 4). This problem could be solved by configuring the DUC and DDC control registers to synchronize the NCOs. Like its predecessor, the program initialized only one receive channel.

Final Transceiver Controller Program

After consultation with application engineers at Pentek, we decided to start from scratch and develop a new controller program using the examples as building blocks. This was partially motivated by the difficulty anticipated in adding multiple receive channel capability to `baseline_uct_demo.c` program – it would not have been a matter of replicating lines of source code to set up additional receive channels. This was because of the way data acquisitions were managed in the Cobalt module. A significant difference was that the new controller program used the ReadyFlow library's built-in functions to load configuration settings to the Cobalt rather than custom written functions as was the case with `baseline_uct_demo` (See Appendix A).

Example programs most closely matching the transmission and digitization requirements were selected from the ReadyFlow examples folder. They were:

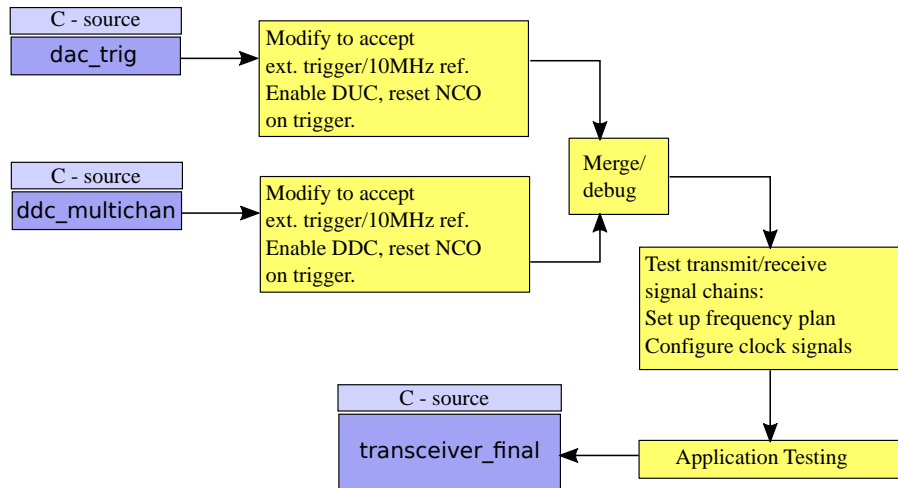


Figure 3.3: Development flow for the final controller program. Two example source files, `ddc_multichan` and `dac_trig` were modified to accept a 10 MHz reference and initiate using external triggering. Numerically controlled oscillators in transmit and receive chains were configured to reset phase on external trigger events. By joining these two files, the digital transceiver controller source code was finally produced after extensive testing and development during a three week support visit to Pentek.

dac_trig: Simple DAC waveform output from memory using a single channel linked list controller.

This program did not use the digital upconverter on the DAC5688.

ddc_multichan: Demonstrated the capability of three DDC IP cores for digital down-conversion of an input data stream from multiple ADCs.

These were then modified to incorporate the necessary board resources and configured to work with an external trigger and frequency reference. In this way, most of the development work for transmit and digitization was done in separate programs. To merge the transmitting and receiving controller codes was the next logical step. It may have been possible to run the two programs in parallel on the same board, however this approach was abandoned because many board resources were shared between the programs, invariably leading to conflicts. The merged program was then refined to the point where it would successfully compile. A debugging tool embedded in the integrated development environment was indispensable for getting this right. It then systematically tested and tweaked until in-phase, low-jitter waveforms could be generated using the digital upconverter. Next, multi-channel digitization using the digital downconverters was tested. Loop-back measurements were done to ensure that identical transmitted pulses resulted in identical recorded waveforms on all receive channels.

3.2.2 Digital Waveform Representation

The theory underlying pulsed radar signal generation and quantization is well documented by Richards [13]. The Cobalt module implements a digital I/Q sampling system in its receiver chain, which is com-

Table 3.2: Cobalt Controller Program Versions and Capabilities

Property	baseline_doppler_demo	baseline_uct_demo	ddc_multichan
DUC complex multiplier enabled?	Yes , 55 MHz	Yes, 90 MHz	Yes, 125 MHz
DDC complex multiplier enabled?	No	Yes, 55 MHz	Yes, 55 MHz
External triggering?	Yes	Yes	Yes
10 MHz reference clock used?	No	Yes	Yes
Coherent generation and digitization?	Yes (real samples)	No	Yes
Number of ADC channels available	One	One	Three
DAC output sample rate (MSPS)	200	360	720
DAC interpolation	2x	2x	4x
ADC digitization sample rate (MSPS)	200	180	180
ADC decimation	0x	2x	2x

mon in modern radar systems. A brief overview of mathematical expressions for the linear frequency modulated (LFM) pulse and digital representations of the baseband waveforms are given here. A linear frequency modulated pulse is defined by Skolnik et al [14] as

$$x(t) = A \text{rect}(t/T) \cos \left[2\pi f_0 t + \frac{\pi B}{T} t^2 \right] \quad (3.1)$$

where f_0 is the carrier frequency, T the pulse duration, B is the bandwidth. The $\text{rect}(t)$ function is defined as

$$\text{rect}(t) = \begin{cases} 1, & |t| < 1/2 \\ 0, & |t| > 1/2 \end{cases} \quad (3.2)$$

The complex baseband data for the LFM chirp is generated using the following expression:

$$x_a(t_n) = \exp(\pi(B/T)t_n^2 j) \text{rect}(t_n/T) \quad (3.3)$$

The above equation represents a complex valued up-chirp at discrete times $t_n = n T_s$, where the sample period is T_s . In the Cobalt's DDR3 memory each sample is stored as a 32-bit value, the most significant 16 bits store the real component, the rest imaginary. The complex multiplier in the DAC5688 introduces carrier frequency $f_0 = 125$ MHz, producing the complex signal:

$$\begin{aligned} x_a(t_n) &= \exp(2\pi f_0 t_n j + \pi(B/T)t_n^2 j) \text{rect}(t_n/T) \\ &= I(t_n) + j Q(t_n) \end{aligned} \quad (3.4)$$

I(t) and Q(t) are the in phase and quadrature signals respectively and are output on the DAC5688 I and Q channels, which together form an analytic version of the output spectrum. All the spectral information is available from either channel. The REX accepts/generates single real valued IF signals only. All the spectral content in the transmit signal is available from either of the DAC5688 output channels, so only one is used to drive the REX IF input. The IF signal at each channel of the DAC5688 will contain replicas of the spectrum at multiples of the output frequency [15], low-pass filtering removes these components.

In a loop-back measurement, the input waveform at the A/D channel input is given by equation 3.4. After quantization and down-conversion the received signal is represented equation 3.3.

3.2.3 Transmit Chain

The Cobalt is equipped with a Texas Instruments DAC5688 D/A module. The DAC channel 1 output drives the single REX IF input, which is then upconverted, amplified, and transmitted. The second DAC channel is unused and terminated by a 50 Ω load. The REX will upconvert the IF input to only one of its output channels at a time. A block diagram of the Cobalt SDR transmitter is shown in Figure 3.4 on page 31. The 125 MHz REX IF input requires that we use the digital upconverter (DUC) on the Cobalt's DAC5688 in order to generate waveforms at a 125 MHz center frequency. Without the upconverter, the IF can not be reached by the DAC as the maximum rate at which samples can accessed from memory is 250 MSPS, limiting the output frequency to 125 MHz by the Nyquist criterion. The DAC5688 incorporates interpolation filters and a full complex multiplier with a digital local oscillator. These two components make it possible to maintain the information bandwidth of the signal whilst transmitting at frequencies much higher than 125 MHz. An excellent explanation of the up-sampling of the input data stream is given by Lyons [16]. Also included in the DAC5688 (but not shown in Figure 3.4) are a Quadrature Modulator Correction block and an inverse-sinc filter.

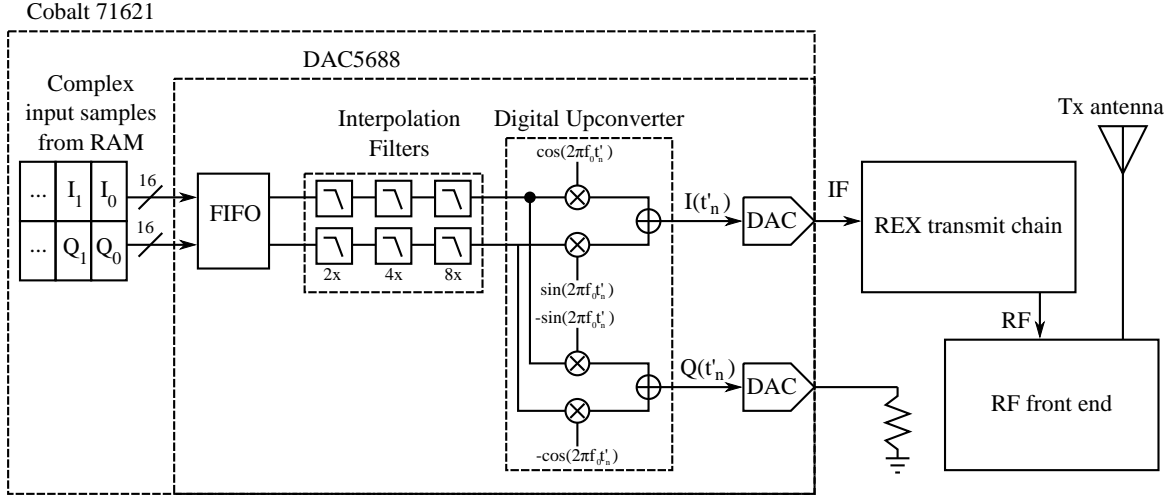


Figure 3.4: The simplified software defined radio transmitter. This diagram shows the upconversion process from digital storage to RF. The maximum rate at which data can be loaded into the FIFO is 250 MSPS.

The pre-installed waveform generator on the Cobalt's FPGA feeds the complex-baseband data to the DAC5688, which handles the digital upconversion on its own. The numerically controlled oscillator generates the real and imaginary components of $\exp(2\pi f_0 t_n j)$ at a rate equal to the DAC output frequency. The DAC5688 FIFO data input and DAC output rates are related by the interpolation rate:

$$F_{\text{DAC}} = F_{\text{data}} \times \text{Interpolation Rate} \quad (3.5)$$

By selecting an input data rate of $F_{\text{data}} = 180 \text{ MHz}$ (for reasons explained in Section 3.2.4), together with an interpolation factor of 2, an output sample rate of $F_{\text{DAC}} = 360 \text{ MHz}$ is set. Frequencies just under $F_{\text{DAC}}/2 = 180 \text{ MHz}$ can be generated from either the I or Q DAC outputs in this way. The output spectrum is repeated at multiples of the DAC sample rate, F_{DAC} . Spectral components will therefore be present from 230-280 MHz. If the interpolation rate is then doubled to 4, it will increase F_{DAC} to 720 MHz and move the repeated spectrum to much higher frequencies. This relaxes filtering requirements to remove the spectra. The frequency plan to achieve this is shown in Figure 3.5.

It is important to note that the digital local oscillator phase in the DAC can be set to any value using software interrupts or by an external trigger edge. A block diagram of the numerically controlled oscillator which generates the sine and cosine terms for the multiplier is shown in Figure 3.6. The consistent phase of transmitted pulses can be guaranteed by resetting the local oscillator phase to zero, precisely when the external trigger goes high. Phase resets via external triggering are not a default configuration and careful setup is required to achieve them. The exact value of the frequency increment register is calculated by functions in the ReadyFlow package, so there is no need for the programmer to directly assign its value. The phase offset is left at its default value of zero.

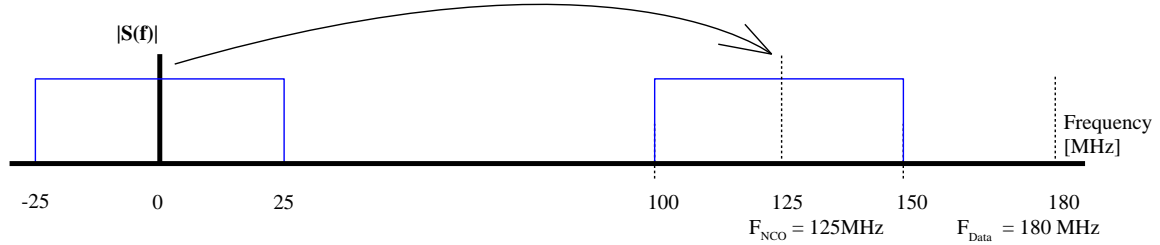


Figure 3.5: Digital upconversion from complex baseband to the 125 MHz IF. The complex spectrum magnitudes represented here are of analytic signals generated from complex samples stored on the DDR3 RAM on the Cobalt module. The baseband spectrum is translated to the IF by multiplication with sine and cosine terms generated by the numerically controlled oscillator and output at the DAC frequency. Note that the sample rates of the input data spectrum at baseband is 180 MHz, interpolation filters in the DAC will increase this by a factor equal to the interpolation factor to generate output at the F_{DAC} frequency.

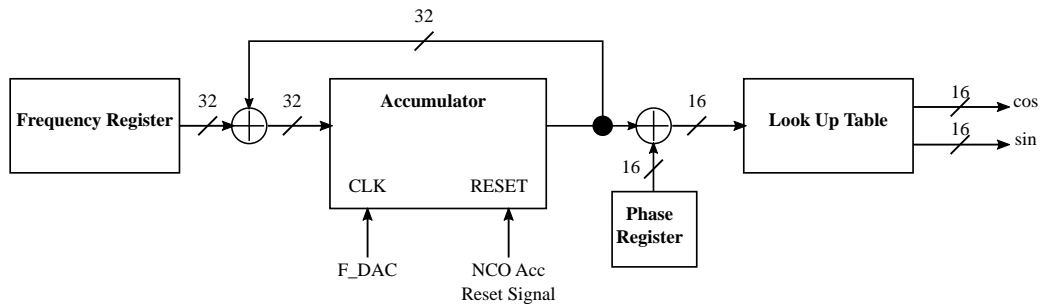


Figure 3.6: The DAC5688 numerically controlled oscillator block diagram. The accumulator is reset via the *NCO Acc Reset Signal*. The F_{DAC} is the DAC output frequency clock which is equal to the data input rate times the interpolation factor [17]. Note that the multiplication operation occurs after the interpolation filters in the signal processing chain, so that the look up table is actually being accessed at a rate equal to the DAC output frequency.

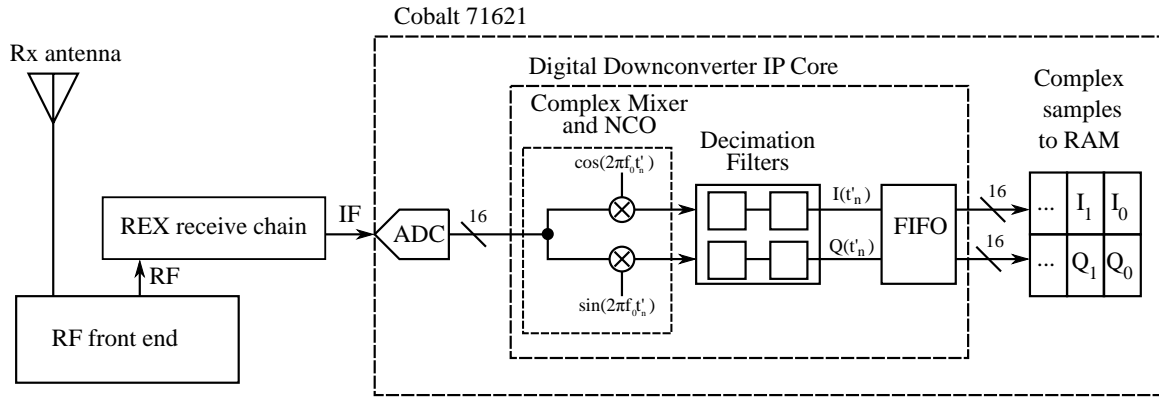


Figure 3.7: The simplified software defined radio receiver chain. This shows the signal chain from RF to digital storage. The quadrature channel is generated internally using the complex multiplier and numerically controlled oscillators in the DDC IP core on the FPGA. The phase of the NCO was configured to reset on external trigger events to ensure repeatable phase behaviour, just as with the DAC5688 NCO accumulator in Figure 3.6.

3.2.4 Receive Chains

The SDR receiver chain is described here. A block diagram of the SDR receiver is shown in Figure 3.7. The down-conversion is facilitated by IP cores pre-installed on the Cobalt FPGA. The three receive channels on the Cobalt are each transformer-coupled to a Texas Instruments ADS5485 A/D converter, which has a maximum sampling rate of 200 MSPS. The active node uses all three receive channels on the Cobalt, each one connected via coaxial cable to a REX IF output.

The Cobalt FPGA IP core implements three digital down converters - one per receive channel. Each DDC IP core incorporates a digital mixer and local oscillator, and a decimation filter. The local oscillator frequency is numerically controlled and its phase can be reset on external trigger events just as with the digital upconverter. If local oscillators on the DDC channels are configured to set their phases to zero on each external trigger event, phase variation will not be introduced by the down-conversion chain.

The incoming IF signal is centered on the 125 MHz carrier and sweeps from 100 to 150 MHz. An undersampling approach is therefore required. Selecting an ADC clock of 180 MHz creates a second Nyquist zone from 90 to 180 MHz, leaving enough space for the chirp spectrum. A decimation factor of 2 results in an effective complex sampling rate of 90 MHz, which satisfies the Nyquist criterion for complex sampling and is adequate for the 50 MHz chirp bandwidth. This frequency translation is shown in Figure 3.8. Note that this flips the spectrum – an up-chirp will become a down-chirp. Thus, the numerically controlled oscillator of the DDC on the Cobalt FPGA IP core is tuned to 55 MHz and will downconvert IF chirp to complex baseband. Lyons [16] provides insight to the quadrature sampling and decimation processes that are implemented in the Cobalt module. The spectrum is also reversed by this process to ensure that up-chirps at IF are downconverted to baseband up-chirps.

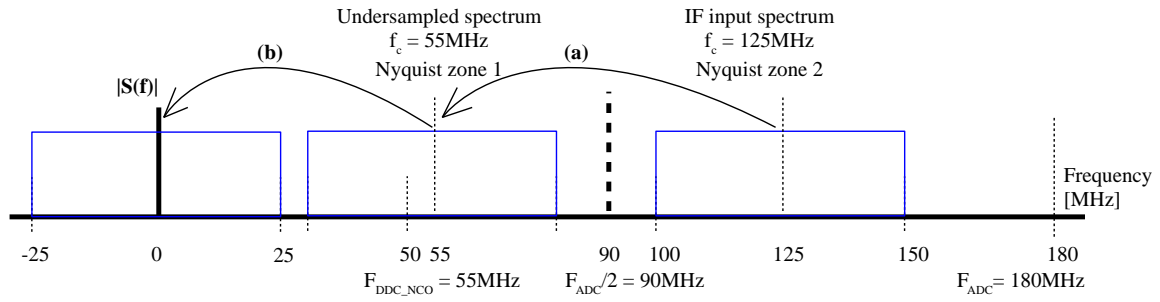


Figure 3.8: The digital down-conversion frequency plan for a real 50 MHz bandwidth LFM pulse from the REX. The incoming 125 MHz IF signal is undersampled at 180 MHz, producing folding from the second Nyquist zone to the first (a). This produces a frequency centered on 55 MHz. Digital down-conversion generates a complex signal from the stream of real input samples and translates the spectrum from 55 MHz to complex baseband (b). A decimation factor of 2x results in an complex sample rate of 90 MHz for the real data which is written to system memory via the PCIe interface on the FPGA.

Each complex sample is stored as a 32-bit word, the 16 most significant bits being the in-phase component, and the 16 least significant being the quadrature part. The downconverted waveform data were written to the hard drive was from ADC1 when recording L-band, or from ADC2 and ADC3 together when recording polarimetrically in X-band. The data were recorded in one file per channel on the Cobalt host computer during a measurement.

3.2.5 Laboratory Test Equipment Setup

The setup for a loop-back measurement is shown in Figure 3.9, which shows the DAC output being low-pass filtered and then fed into an IF splitter to drive all three ADC channels. The DAC and ADC channels were connected to 1 m sections of CNT-100 50 Ω braided coaxial cable, manufactured by CommScope. The Cobalt front panel uses SSMC connectors. During testing, the frequency distribution and timing control units were mimicked by a laboratory signal generator and an arbitrary waveform generator respectively.

Variations of the configuration in Figure 3.9 were used for acceptance tests. For example, to measure DAC output only, the output was connected to an Agilent FieldFox model N9912A RF analyzer. Digitization was tested by driving the splitter with a sine wave from an Agilent E4400B ESG signal generator, with and without the digital downconverter enabled.

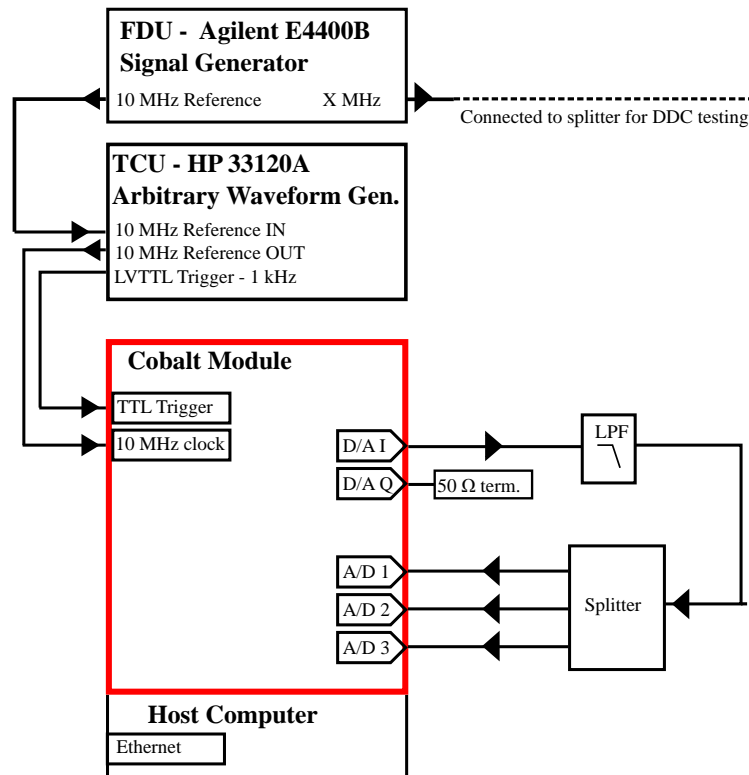


Figure 3.9: Measurement setup used for loop-back testing. Only the output of DAC 1 on the Cobalt module was used. Different models of Signal and Arbitrary Waveform Generators were used during testing, depending on what was available. To test digitization, the Agilent E4400B generator supplied a sine wave to the signal splitter, which provided three near-identical sine waves for multi-channel digitization tests. In loop-back configuration, the DAC I output was low-pass filtered and fed directly to the splitter. It is was important to phase-lock the internal oscillators of the FDU, TCU, and the Cobalt via 10 MHz reference signals. Typically the reference from the E4400B was used to supply this signal. The AWG supplied the LVTTL trigger signal to the Cobalt trigger input, and could be programmed to supply a finite number of pulses. The Cobalt module was programmed by the host computer, which was equipped with the necessary drivers to initialize the board.

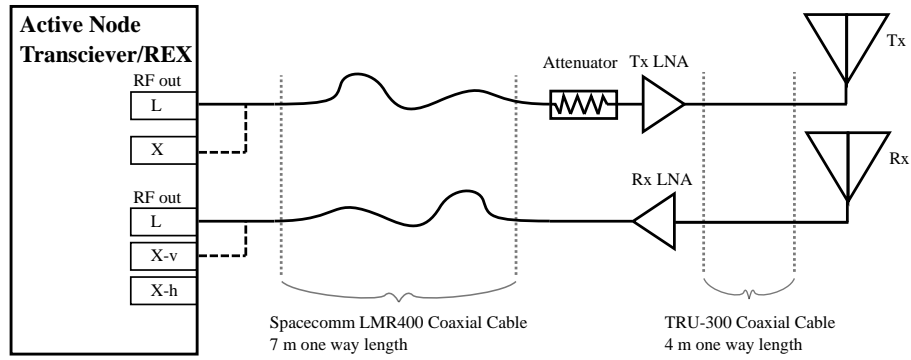


Figure 3.10: The RF frontend components in the active node prototype consist simply of the receiver exciter, coaxial cables, RF amplifiers and attenuators and antennas.

3.3 Medium-Power Prototype Implementation

Building a low powered prototype radar was beyond the scope of this project. However, it was important to verify that the digital transceiver could function as part of a coherent radar system. Moreover, much could be learned about the behaviour of the digital transceiver in a low powered prototype. Using X- and L-band LNAs (borrowed from the full power RF frontend components) to serve as transmit and receive amplifiers, it was possible to do short range radar measurements to verify that the Cobalt was actually detecting stationary and moving targets. The low transmitting power and short ranges in these rather crude experiments were different from what was planned for the final NeXtRAD active node. However, this does not detract from the usefulness of the measurements in establishing that the digital transceiver works reliably. In terms of digital signal processing, the prototype and final active node are fundamentally the same.

To perform simple low power tests we employed the experimental set up used for the IF loop-back tests shown in Figure 3.9, but with the addition of low noise amplifiers and antennas. These extra components are represented by the dashed box labelled “RF Frontend/Antenna Systems” in Figure 2.3 on page 16. In Figure 3.10, the RF amplifiers and antennas are shown attached to the active node REX by RF coaxial cable. During rooftop testing the digital transceiver and REX were housed in the microwave laboratory, and the power amplifiers and antennas were stationed on the roof. A pair of LMR-400 coaxial cables connected the amplifiers to the REX RF connectors, each approximately 7 m in length. A pair of TRUcore-300 cables connected the transmit and receive amplifiers to their respective antennas on the rooftop, each approximately 4 m long. The attenuator, introduced just before the transmitting amplifier in Figure 3.10 ensures that the incoming signal level from the REX is at about 0 dBm to prevent driving the amplifier into saturation, and to keep harmonic levels low.

Testing was done in single polarization at both X- and L-bands (not simultaneously), which required different amplifiers and antennas. Three different configurations were used to do outdoor testing. The amplifiers and antennas used for each frequency test are given in Table 3.3.

Table 3.3: Prototype Active Node Antennas and Amplifiers.

Test	Band	Tx antenna, beamwidth*	Rx antenna, beamwidth*	Tx Amp, power**	Rx Amp, power**
(a)	L	Reutech “plank”, 6.5°	Same as Tx	ZX60-P162LN+, 19 dBm	Same as Tx
(b)	L	A-LPDA-0020-V2 Yagi, 60°	Same as Tx	ZRL-3500+, 24 dBm	ZX60-P162LN+, 19 dBm
(c)	L	Reflector dish, 10°	Rectangular horn, 20°	ZRL-3500+, 24 dBm	ZX60-P162LN+, 19 dBm
(d)	X	Conical horn, 10°	Same as Tx	ZX60-183A+, 18 dBm	ZX60-14012L+, 11.5 dBm

* Azimuth beamwidth.

** Power at 1 dB compression point, at 1.3 GHz (L-band), or 8.5 GHz (X-band).

All amplifiers manufactured by Mini-Circuits Inc.

The first rooftop test used configuration (a), these were single pulse measurements only. L-band experiments used an L-band printed dipole antenna pair, driven by a split corporate feed from a single input with tapering applied across the aperture. These units were originally used as part of a phased array antenna, and have a 5° azimuth beamwidth. The elevation beamwidth is approximately 60°.

Configuration (b) used two communications antennas which were procured from Poynting Direct. These broadband antennas had a modest 8 dBi gain and were not very directional.

In configuration (c) a reflector dish antenna prototype and a sectoral horn antenna were used for transmitting and receiving respectively, both developed by Paine [11].

For X-band testing we used configuration (d). Identical conical horn antennas developed by Cheng [10] were used for both transmit and receive. The transmitting antennas were selected on the basis of expediency – the only object was to obtain radar data using the newly-programmed digital transceiver. All amplifiers were borrowed from components intended for the high-power RF frontend developed by Stevens [9], except the ZRL-3500+ L-band amplifier which was purchased specifically for these experiments.

3.4 Summary

Not all user requirements specified in Section 2.2.1 for the digital transceiver could not be tested directly. In Section 2.2.1 application test procedures, or experiments, were designed to test sys-

tematically the signal generation and digitization capabilities of the system. These experiments are summarized in Table 5.1. The development of the Cobalt software would follow more or less the same progression as these experiments, as each processing task on the board is configured in C. Some of the user requirements, such as 8, 9, 11 and 12, which called for precise control radar measurements, were not related to high performance signal processing operations. Some familiarity with the Cobalt's features would be sufficient to configure the board to meet these. More intensive signal processing tasks required more careful setup to achieve phase stability on transmit or receive, and to reduce overall system jitter. For these tests careful measurement of the DAC output would be required. Digitization would be tested by supplying known signals to the ADCs and examining the raw recorded data. Loop-back data would be used to determine whether the system could form a compressed response consistent with theory, and whether the system was able to consistently digitize waveforms without phase drift from pulse to pulse.

A detailed overview of the Cobalt module is given in Section 3.2. To develop controller programs the ReadyFlow software library is used to configure board resources for different signal processing tasks. The data structures and callable functions in ReadyFlow make the task easier, but the board is highly reconfigurable and with this comes a high degree of complexity. To aid program designers, a set of example programs are provided with the board to demonstrate its capabilities. None of these demo programs would satisfy the user requirements without extensive modification. Several controller programs were developed and tested. This process culminated in the final successful version which met all the DSP related user requirements for the digital transceiver. The final controller program was created by merging two of the example programs, but with significant modifications and configuration changes to both programs in the process. Assistance from the creators of the Cobalt board at Pentek was required to accomplish this.

Mathematical expressions for the generation of the analytic baseband form of the LFM pulse were presented in Section 3.2.2. These made it clear how the waveform data is generated before experiments. The operation of the digital up and down-conversion processes is easily understood in terms of multiplication operations with a complex exponential, bearing mind that the frequencies of the digital local oscillators in the transmit and receive chains are different [18]. The transmit chain of the Cobalt is examined in detail in Section 3.2.3. This is a software defined radio transmitter which translates complex baseband data at relatively low data rates (maximum 250 MHz) to a much greater analogue output sample rate at the DAC (around 800 MHz). A frequency plan taking into consideration constraints on data sample rates and the interpolation factor selected is presented in Figure 3.5. The software defined radio receive chain of the Cobalt is examined in Section 3.2.4. The maximum ADC sample rate is 200 MHz, which dictates that the 100-150 MHz frequency range the Cobalt receives be undersampled at 180 MHz. The I and Q components are generated digitally in this direct IF sampling approach, and a decimation factor of 2x results in an effective sampling rate of 90 MHz. A 90 MHz complex sampling rate is sufficient for sampling the standard 50 MHz bandwidth of the

LFM pulse of NeXtRAD. The receive chain frequency plan is shown in Figure 3.8.

Laboratory equipment for most of the digital transceiver testing consisted of only three main components: (1) The Cobalt module and its host PC, (2) a laboratory signal generator which provided test and reference signals in the 0 -200 MHz range, and (3) an arbitrary waveform generator which was used to supply LVTTTL trigger pulses. These are shown in Figure 3.9. The instruments for reading and measuring the IF signals included spectrum analyzers and oscilloscopes.

The low power prototype was not intended to test the digital transceiver against any of the user requirements per se. It was intended to demonstrate that the Cobalt module was effective in transmitting and digitizing radar signals, when functioning as part of a simple radar system. It was of particular importance to demonstrate that the digital transceiver could interface with the receiver exciter and exchange signals with it via the 125 MHz IF.

Chapter 4

Acceptance Tests

The outcome of acceptance test procedures are documented in this chapter. The results of experiments A through E (see Table 5.1 on page 87) are presented sequentially. The generation of waveforms using the DAC output channel is first presented in Section 4.1. The single and multi-channel digitization of tones generated by the DAC and by a signal generator is tested next in Section 4.2. To verify the phase stability of the transmit and digitization channels when operating in tandem, loop-back measurements were taken as described in Section 4.3. The setup of linked-list engines which independently controlled the transmit and digitization is given in Section 4.4. The acceptance tests conclude with the maximum PRF measurement in multichannel acquisition mode in Section 4.5. The radar measurements taken using the low-powered radar prototype described in Section 3.3 are presented last, demonstrating the ability of the digital transceiver to function roughly as it would in a fully integrated system.

4.1 Experiment A: Waveform Generation

Waveform generation satisfying user requirements was tested using `doppler_uct_demo` and the heavily modified `ddc_multichan`. To transmit the 50 MHz LFM chirp at the intermediate frequency was possible with either one of these controller programs, but the phase stability issue was completely solved by `ddc_multichan` during a support visit to Pentek Inc. in June 2016. The altered `ddc_multichan` was created by merging `dac_trig` into the original code for `ddc_multichan` and debugging the result, as depicted in Figure 3.3 on page 28.

The experimental setup used for these measurements is as shown in Figure 3.9 on page 35.

Phase-stable Sine Wave Generation with `ddc_multichan`

The digital upconverter on the Cobalt employed a numerically controlled oscillator and complex multiplier in the DAC5688 to do frequency conversion. As a result, phase shift is introduced by the digital upconversion process. The complex samples generated by the NCO were therefore more accurately described by $\exp[(\omega_0 t + \phi_r)j]$, where ϕ_r was the NCO phase when the external trigger signal arrived – an unknown value. Therefore equation 3.4 modeling the complex valued LFM chirp at the DAC I and Q output channels actually included the random phase term, viz:

$$x_a(t) = \exp[(2\pi f_0 + \pi(B/T)t^2 + \phi_r)j] \text{rect}(t/T) \quad (4.1)$$

This ϕ_r term would obliterate any hope of successful doppler processing. A similar problem existed in the digital down-conversion where NCOs on the FPGA have a phase that could be any value when the external trigger pulse arrived. Provided that phase shift introduced is constant from pulse to pulse on transmit and receive, successive digitized and downconverted waveforms in a loop-back test will be phase-constant. The same would apply for reflections from stationary point scatterers in the completed radar. However, NCOs in the DDC and DUC were essentially free-running clocks with respect to the external trigger signal. This resulted in apparently random phase of the transmitted signals in the early pulse generation tests¹.

The obvious way to achieve phase-stable, low-jitter output with `ddc_multichan` was to reset the DAC numerically controlled oscillator phase, at every trigger event. After some trial and error with different configuration register settings for the DAC5688, the DAC NCO was successfully reset on the trigger event. This resulted in the phase of the generated waveform being exactly consistent.

DAC output jitter can be described as the variation in delay between the rising edge of the trigger pulse and waveform output, denoted here by $T_{\text{delay_DAC}}$. To put transmit jitter into perspective, consider a 100 MHz sine wave has a period of 10 ns. The transmit jitter of 2.5 ns is equivalent to a phase jitter of $2\pi(2.5/10) = \pi/2$ rad, which is enough to prevent coherent integration of radar pulses. Ideally, there should be no jitter in $T_{\text{delay_DAC}}$ at all, but practically it will be on the order of tens of picoseconds. Whether the jitter appeared as a result of measurement error or because of clock distribution problems within the Cobalt module itself was initially unclear.

To simplify the debugging process both DAC and ADC clock frequencies in the Cobalt were set equal to 200 MHz in `ddc_multichan`. The DUC tuning frequency was set to 75 MHz, and an waveform generator on the board was used to produce a 6.25 MHz (that is 200 MHz/32 points per sample). Negative single-sideband digital upconversion would therefore produce a $75 - 6.25 = 68.75$ MHz sine wave at the DAC output channel. The 68.75 MHz output frequency was measured by an Agilent 8562EC spectrum analyzer.

¹See table 3.2 on page 29 for a more informative list of programs developed for the Cobalt board and their capabilities

The first step in eliminating sources of jitter was to create trigger pulses which were precisely synchronized to an external 10 MHz reference clock. A Stanford Research Systems (SRS) model DS345 was used as the arbitrary waveform generator; it supplied both the trigger pulse, and the 10 MHz reference clock from its back panel to the Cobalt reference clock input. The trigger pulse was generated using its arbitrary waveform capability. By assigning the first 8 memory addresses of the Stanford's RAM with values (1, 0, 0, 0, 0, 0, 0, 0), and setting the output sample rate to 10 kHz, a $10 \text{ kHz}/8 = 1.25 \text{ kHz}$ pulse signal was generated. The jitter of the rising edge of this pulse was measured using a Tektronix Model TDS 3032 oscilloscope. It was found to be below 500 ps between subsequent rising edges of the function output. The SRS generator output was split and used to drive both the Cobalt and oscilloscope triggers, allowing fairly accurate measurement of the output delay. In fast trigger mode the scope can measure time differences of 40 ps, but the smallest readable difference from the display is about 200 ps at full bandwidth, i.e. about half a fine division on the display.

By using the Stanford generator as the external trigger supply, the source of jitter in $T_{\text{delay_DAC}}$ could be traced more easily. The two signal probes of the Tektronix 3032 oscilloscope were connected to the SRS function generator output and the Cobalt DAC. The SRS generator's output was used to trigger the oscilloscope acquisition. By using the Cobalt internal clock without referencing it to the Stanford generator 10 MHz reference, 12 ns total variation in the output waveform with respect to the trigger was produced, as viewed on the oscilloscope. The jitter was reduced to about 3.2 ns after connecting the 10 MHz reference from the Stanford back panel to the Cobalt front panel clock input. These two results are shown in figure 4.1. The Cobalt board was able to detect the 10 MHz reference and synthesize the 200 MHz board clock rate from it. In the absence of the reference signal, the board would generate a clock internally using an on-board Silicon Labs Si571 voltage controlled oscillator. Evidently, the unsynchronized internal clocks of the Cobalt and Stanford generator introduced significant jitter of the DAC waveform when viewed on the scope. Why exactly this happened can be understood by analysis of the clock signals in the Stanford and Cobalt, but the final system would not use such a configuration so this analysis was not done.

It was suspected that the CDC7005 clock synthesizer on the Cobalt board was generating 3.2 ns of jitter in Figure 4.1. To overcome this it was possible drive the board clock directly using a 200 MHz, 1 dBm input signal from an HP model 8648D signal generator. A small change in `ddc_multichan` enabled this. The SRS generator was still used to supply the trigger signal and its timebase was driven by the HP 8648D 10 MHz reference, thus ensuring a common source clock for the 200 MHz board clock and the trigger signal. After re-running the experiment with this new configuration, in a phase jitter of 3.2 ns on the oscilloscope display resulted – no visible improvement. This meant that jitter in the DAC output signal was not measurably different when using a 10 MHz clock reference or when using a 200 MHz signal to directly drive the board clock.

The remaining source for apparent trigger jitter of the Cobalt DAC output was likely due to the PLL in the SRS generator. By triggering the scope on the SRS-generated trigger signal, jitter from its

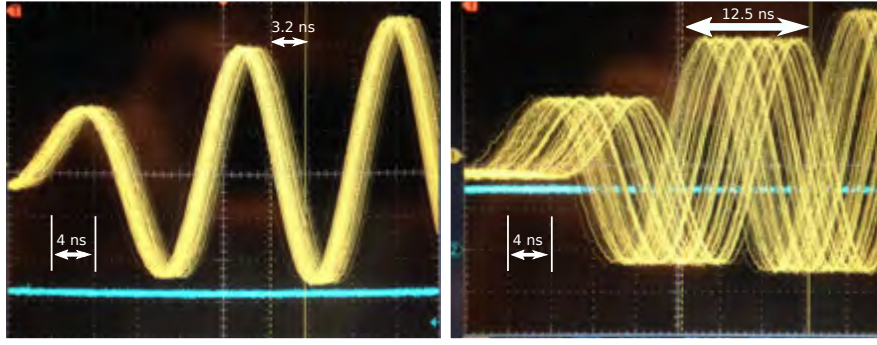


Figure 4.1: Tektronix 3032 oscilloscope display of the DAC waveform with (left) and without (right) the 10 MHz reference signal supplied to the Cobalt, showing the first few cycles of the waveform at a 1.25 kHz PRF. Trigger supplied by the AWG, oscilloscope acquisition triggered by the same signal (blue trace). The output waveform frequency is 68.75 MHz. Digital phosphor shows traces of multiple transmitted waveforms. The spread of equi-phase points the waveforms gives an indication of jitter in $T_{\text{delay_DAC}}$

PLL would be introduced to the scope display which manifested as jitter of the Cobalt DAC output. To circumvent this the Cobalt was configured to *supply* an LVPECL trigger signal from its sync bus output on the front panel. In this way, the internal trigger signal from the Cobalt could be used to trigger the scope acquisition, giving a very accurate indication of how precisely timed waveform generation was with respect to the internal trigger signal. The Cobalt was still dependent on the trigger from the Stanford, but the scope was triggered from a signal within the Cobalt itself. The Gate B+ trigger signal was routed to pin A9 of the 26 pin sync/gate connector on the Cobalt, see section 2.7.4 of [12] for details. The output waveform jitter as measured by the scope was reduced to approximately 280 ps, as shown in Figure 4.2. A 10 MHz external clock reference was used. These measurements showed that $t_{\text{delay_DAC}}$ jittered by less than 300 ps. Output jitter could be established more accurately by statistical analysis of the oscilloscope data, but the sub-nanosecond jitter was less a DAC output clock cycle of $1/200 \text{ MHz} = 5 \text{ ns}$.

The test frequency was 68.75 MHz as opposed to one in the 100 - 150 MHz range which REX would require. However, the output jitter would not have been greatly affected by increasing the interpolation rate, NCO frequency, or DAC output frequency. One problem that was not resolved was a 1-clock cycle variation in the delay between the trigger pulse and the output waveform. Once triggered, the delay between trigger and waveform output, $T_{\text{delay_DAC}}$, was essentially jitter-free at the 1.25 kHz PRF. However, in consecutive runs of the program there was a variation of 1 sample of the DAC, i.e., output delay was either $T_{\text{delay_DAC}}$ or $T_{\text{delay_DAC}} + T_s$, where $T_s = 1/F_{\text{DAC}}$ was the DAC output sample clock period. This was observed at an interpolation rate of 2x. Similar oscilloscope measurements of the output taken at a 4x interpolation rate showed that the output delay could take on 4 discrete values: $T_{\text{delay_DAC}} + n T_s$, where n was 0, 1, 2, or 3. As before, once the output had started and the trigger was arriving at the PRF, no DAC sample period jitter was visible in the output. Given that

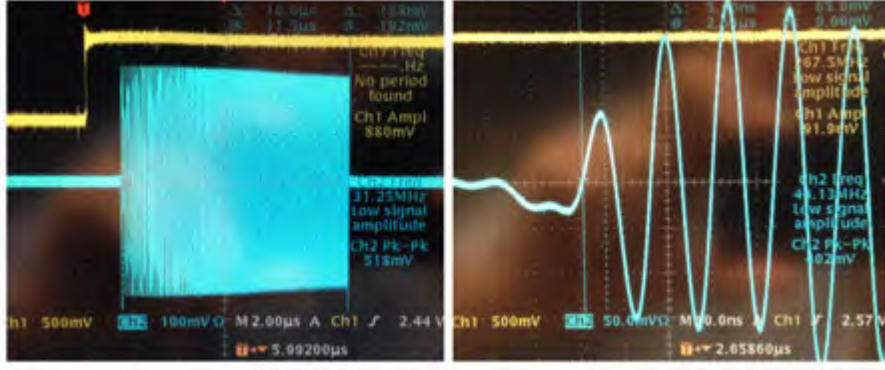


Figure 4.2: The LVPECL (yellow) and DAC output (blue) waveforms as captured by the Tektronix 3032 oscilloscope. The LVPECL trigger signal is generated in the Cobalt's FPGA and is directly linked to the DAC output gate signal. This gives a much more accurate representation of the relative timing between the trigger signal arrival and the DAC waveform output.

the delay was always consistent once the board was running and that this would not have an impact on post-processing, run-to-run jitter was not eliminated. It was likely that the problem originated in the CDC7005 clock synthesizer on the board. This component contains several clock dividers, which were configured to supply a high frequency clock to the DAC5688, and divided versions of it to the ADC and FPGA IP cores. Unpredictability in the relative delay between rising edges of these sub-divided clock outputs could potentially introduce variation in DAC output delay by multiples of a clock cycle.

LFM Pulse Generation

The first successful IF chirp generation tests were done with `baseline_doppler_demo`. As with the sine wave generation experiments, equipment was configured as in Figure 3.9 on page 35.

The magnitude spectrum of an LFM chirp with bandwidth B at baseband can be approximated by the following expression [14]:

$$|U(f)| \approx \frac{f}{B} \quad (4.2)$$

This approximation works well for LFM waveforms with time-bandwidth products (τB) greater than 50. For smaller time-bandwidth products the approximation deteriorates and ripples begin to appear in the spectrum. The bandwidth is taken at the -6 dB points, which occur close to $\pm B/2$ [19], i.e. the spectral width is between frequencies where

$$20\log_{10}|U(f)| = -6 \text{ dB} \quad (4.3)$$

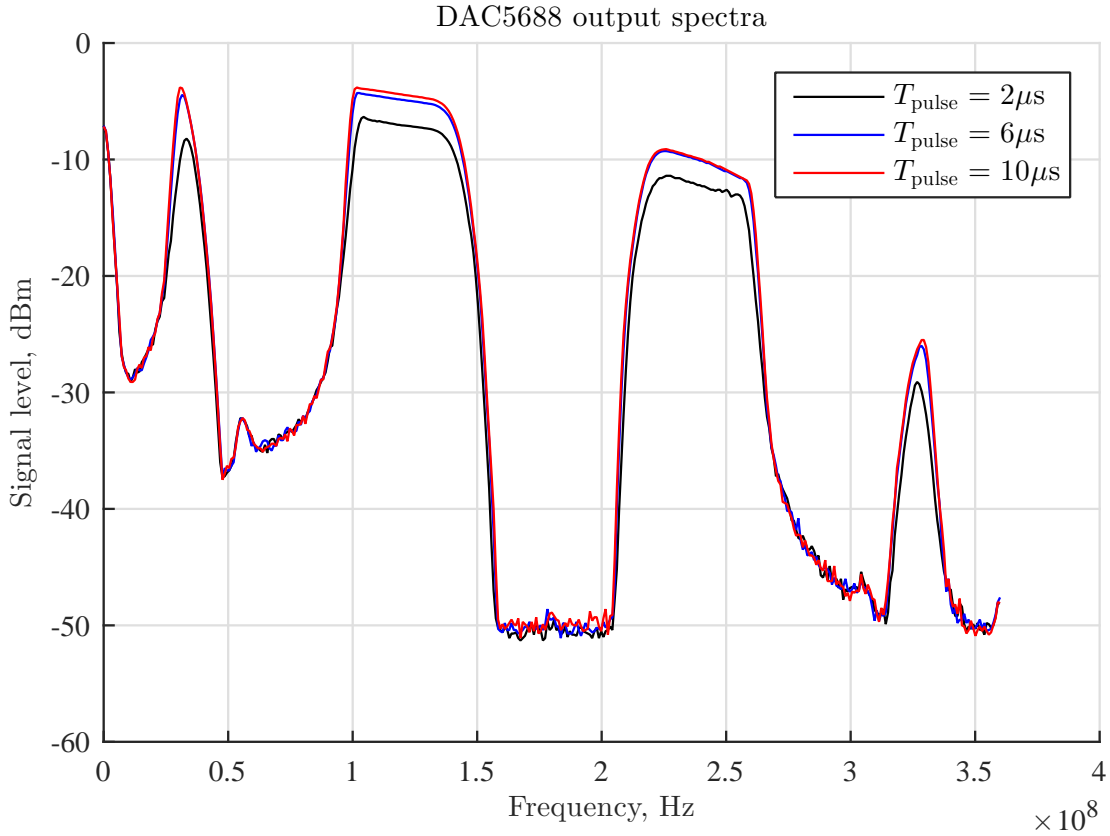


Figure 4.3: The IF output of the Cobalt using the 70 MHz IF for input data waveforms, and a 360 MHz DAC output frequency with interpolation 2x. Pulse lengths of 2, 6, and 10 μs were generated, and the output measured using a Fieldfox N9912A spectrum analyzer. This shows attenuation of frequencies near 150 MHz caused by the FIR1 interpolation filter in the DAC5688. This matches rolloff of the FIR1 filter (see Figure 4.4), a direct result of an injudiciously selected carrier frequency for the waveform data. Also visible is the aperture distortion of the DAC, which resulted in the approximately linear decrease in signal level from 100-130 MHz.

By using `baseline_doppler_demo` to set the board clock frequency to 180 MHz and with 2x DAC interpolation, output frequency of 360 MHz was created. The first attempt at generating waveforms at the IF was done using a 70 MHz center frequency for digitally generated chirps and sine waves. By tuning the NCOs in the Cobalt upconverter to 55 MHz, an output waveform would be centered on a frequency of $55 + 70 = 125$ MHz, assuming positive single-sideband upconversion were implemented. This produced an output spectrum shown in Figure 4.3. A range of pulse lengths were used for the LFM chirp, each with bandwidth 50 MHz, and the spectra recorded by an Agilent E4407B spectrum analyzer. The Cobalt module was programmed using `baseline_doppler_demo` to generate a single pulse per external trigger event for an unlimited number of triggers. Several hundred pulses were supplied by the HP 33120A function generator before the spectrum was fully built up by the E4407B spectrum analyzer. These recordings are plotted in Figure 4.3.

There were two obvious problems with the output in Figure 4.3. Firstly, from 100 to 135 MHz was not

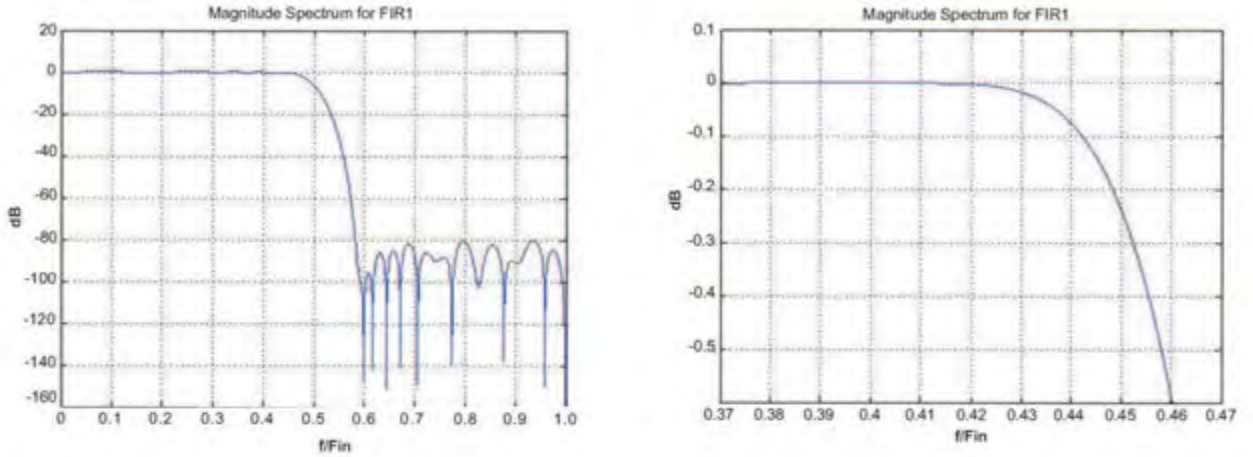


Figure 4.4: The DAC5688 interpolation filter 1 characteristic; magnitude spectrum (left), transition band (right), taken from [17]. This is the filter responsible for creating 2x interpolation. This filter will significantly attenuate frequencies above $0.44F_{\text{data}} = 0.44(180 \text{ MHz}) = 79.2 \text{ MHz}$ in the input data. The result of this attenuation is seen in Figure 4.3, where the input data chirp ranged from 45 to 95 MHz. The solution was to use lower carrier frequency, such as 35 MHz (Figure 4.5), or simply generate the samples at complex baseband with 0 Hz center frequency, which was ultimately used in this project.

level due to the aperture distortion of the DAC. This was remedied by enabling the inverse sinc filter in the DAC, which applied a $f/\sin(f)$ weight to the output spectrum. Secondly, 135 MHz to 150 MHz the spectrum appeared to attenuate more rapidly than could be accounted for by the aperture distortion or by loss in the cables connecting the DAC to the spectrum analyzer. The CNT100 cables would account for only 0.2 to 0.3 dB loss from 100 to 150 MHz according to the cable datasheet. It was suspected that an interpolation filter in the DAC5688 could be responsible for the signal attenuation around 150 MHz. The DAC5688 datasheet [17] showed that the 2x interpolation filter has a characteristic curve shown in Figure 4.4. This filter characteristic matches closely ADC output spectrum in Figure 4.3. The FIR1 frequency response caused attenuation of the higher frequency components of input chirp spectrum.

Selecting a 35 MHz intermediate frequency for the complex samples of the pulse avoided the -3 dB point of the interpolation filter. These data samples fed to the DAC would be interpolated by a factor of 2 and delivered to the complex mixer at twice the data input rate. The frequency plan using the 35 MHz IF is shown in Figure 4.5. The DAC5688 complex mixer NCO was then set to 90 MHz which produced a 125 MHz centred chirp spectrum as shown in Figure 4.6. Also apparent is the mirror image of this spectrum around 180 MHz (which is half the DAC frequency) in the third Nyquist zone from 210 to 260 MHz. These and other higher frequency spectral components exist as a natural consequence of the DAC output sampling. However, these out-of-band frequencies are attenuated by an internal band pass filter in the IF exciter stage of REX [8]. The IF spectrum in Figure 4.5 is as predicted by equation 4.2 showing none of the attenuation from 135 to 150 MHz.

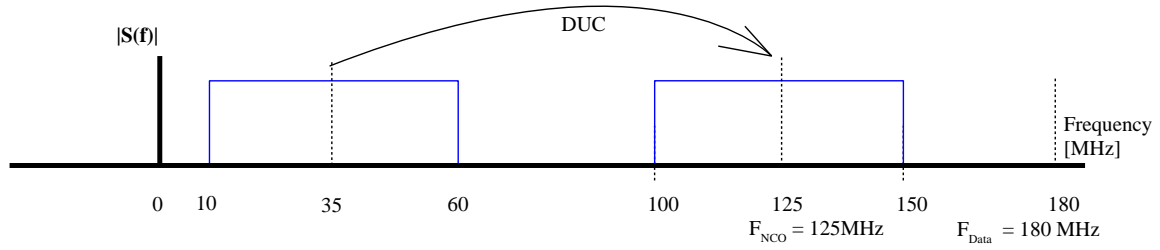


Figure 4.5: A frequency upconversion plan using a 35 MHz carrier for the generated samples. Using this frequency plan and an output frequency of 360 MHz generated the spectrum seen in Figure 4.6. This frequency plan avoided the DAC5688 FIR1 filter rolloff, which is shown in Figure 4.4.

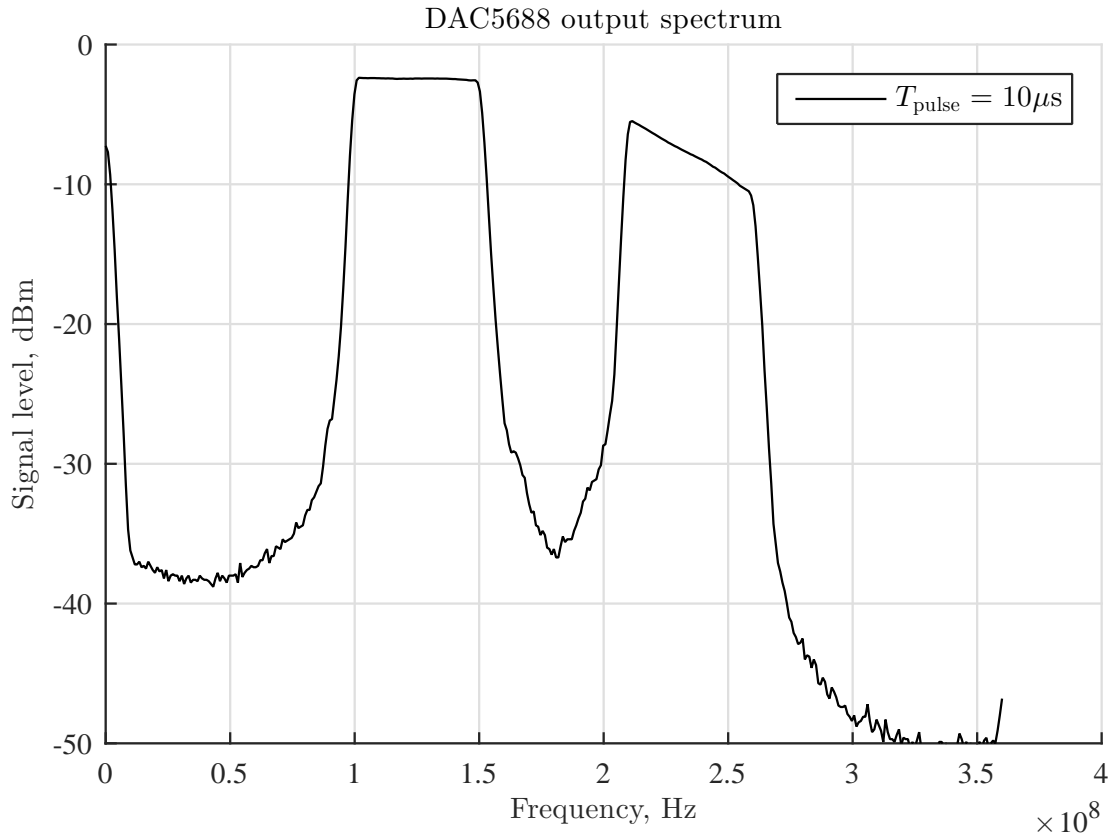


Figure 4.6: The IF output spectrum of a 10 μ s, 50 MHz bandwidth LFM pulse using a 35 MHz carrier on the input data waveform, as shown in the frequency plan in Figure 4.5. Data acquired using a Fieldfox N9912A spectrum analyzer. The DAC aperture distortion correction filter (inverse sinc) was active in this measurement, which produced the flat power level in the 100-150 MHz bandwidth of interest. The NCO frequency was tuned to 90 MHz, interpolation factor 2x, output frequency 360 MHz. The FIR1 2x interpolation filter has not degraded the output spectrum in the 100-150 MHz bandwidth. Also visible is the negative sideband of the spectrum from 210 to 260 MHz, which the repeated output spectrum centered on the 360 MHz DAC output frequency. This is not of concern as out-of-band components are removed filters in the REX. Similar output spectra can be obtained by generating the input data at complex baseband, as seen in Figures 4.7.

The frequency plan used in the final controller program, `ddc_multichan`, used an NCO frequency of precisely 125 MHz as shown in Figure 3.5 on page 32. This plan was decided on after taking into account the effect of interpolation FIR filters on the input data spectrum. The baseband signal does not have the conjugate symmetric spectrum of real signals as it is complex-valued. The IF after upconversion is therefore determined only by the NCO tuning frequency with no need to generate the input data at a lower carrier frequency as is the case in Figure 4.5. This makes it possible to use a higher interpolation rate without sacrificing any information bandwidth in the 50 MHz LFM chirp.

The DAC output sample rate would ideally be as high as hardware constraints allow. This had some implications for the clock distribution on the board, which are discussed in Section 4.3. One advantage of a higher DAC output frequency would be that the replicated spectrum of the DAC in the second Nyquist zone would be easier to filter out. If the full complex output of the DAC5688 were being used, it would be possible to generate complex output waveforms with frequencies almost equal to the output sample rate of the DAC. However, although digital I/Q sampling was implemented by the board only one output channel of the DAC was used to generate a real-valued chirp at the IF. This limited the DAC output waveform frequency to half DAC output frequency.

The DAC output frequency was tested 360 MHz and 720 MHz, with the interpolation factor set to 2x and 4x respectively. The DAC5688 FIFO data input and DAC output rates are related by equation 3.5 on page 31. Input data is generated as complex samples at a 180 MHz sample rate and stored as a waveform file. The waveform generated was the standard 50 MHz bandwidth, LFM chirp at complex baseband. The upconverter NCO was tuned to 125 MHz. The DAC output spectrum for the 720 MHz sample rate is shown in Figure 4.7, which shows the output spectral components mirrored around the half-sample rate of 360 MHz on the left, and the output filtered by a Mini-Circuits VLF-225 low-pass filter. This was the finally decided upon frequency for the DAC. A close-up view of the spectrum is shown in Figure 4.8. This shows that the 3 dB bandwidth of the LFM chirp is indeed 50 MHz on the 125 MHz IF, satisfying the user requirement.

4.2 Experiment B: Waveform Digitization

The ability of the Cobalt module to digitize and downconvert incoming signals with predictable phase was the aim of these measurements. The experimental setup was as shown in Figure 3.9 on page 35. The Agilent E4400B ESG series generator was used to generate the test sine wave and the 10 MHz reference signal (from the back panel) to the digital transceiver board. An HP 33120A Arbitrary Waveform Generator supplied the trigger signal.

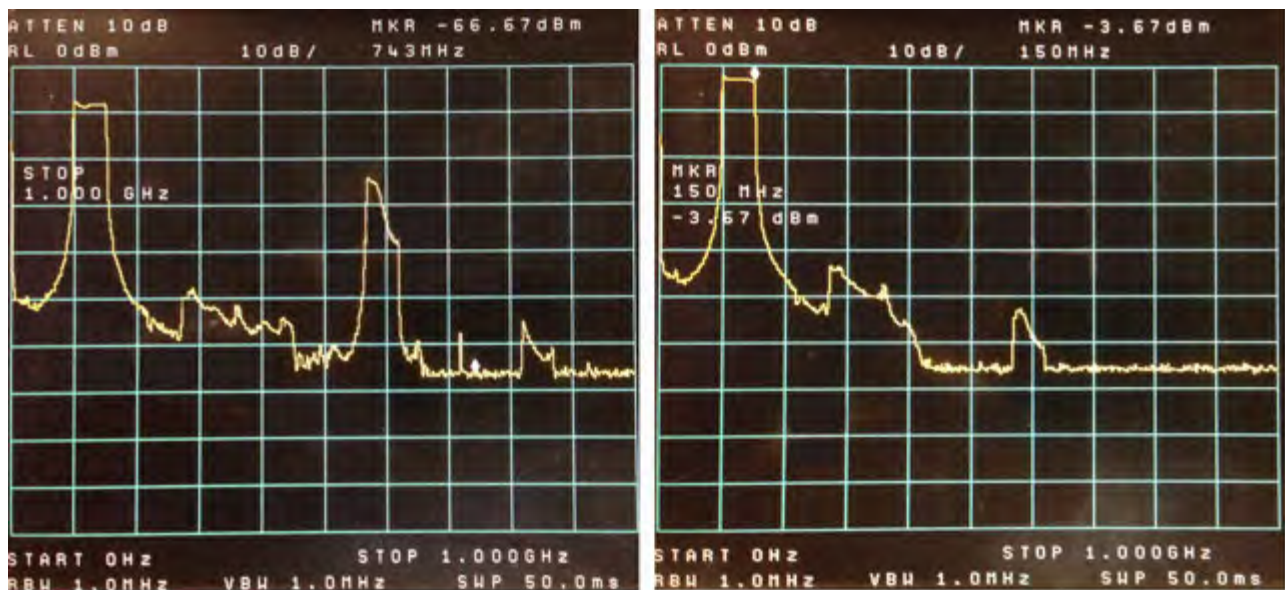


Figure 4.7: The DAC output spectrum generated using the final version of `ddc_multichan`. Output frequency: 720 MHz, interpolation 4x. The unfiltered output on left, and low-pass filtered on right. The input data is centered on 0 Hz, as suggested in the frequency plan in Figure 3.5. The interpolation filters do not significantly attenuate any portion of the output spectrum from 100-150 MHz.

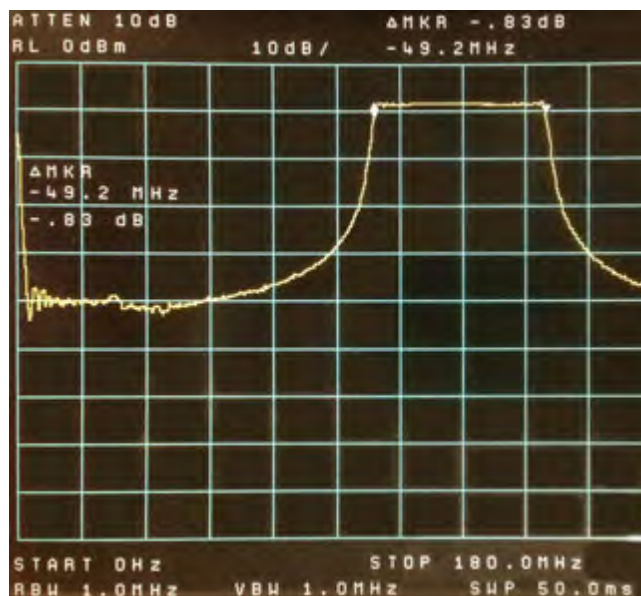


Figure 4.8: The output spectrum of the 125 MHz IF LFM chirp with 50 MHz bandwidth, generated by the finalized transmit chain configuration in `ddc_multichan`. The DAC output frequency is 720 MHz, interpolation rate 4x.

4.2.1 Exp. B.i: Digitization of Sine waves

The program used to do this experiment was `baseline_uct_demo`, which enabled the DDC IP cores on FPGA.

The frequency plan used for the digitization experiment was presented in Section 3.2.4. Each of the Cobalt's ADC channels use a Texas Instruments ADS5484/5 with a 200 MSPS maximum sampling rate. This maximum sampling rate dictates that an undersampling approach be used to digitize the 125 MHz IF signal incoming from REX. The signal is thus sampled in the 2nd Nyquist zone; frequencies between $F_s/2$ and F_s , where $F_s = 180$ MHz. This results in the spectrum folding down to a center frequency of 55 MHz, which is the frequency set on digital downconverter NCOs. This translates spectral components centered on 55 MHz to a 0 Hz.

To test digitization of an undersampled test tone in the second Nyquist zone of the ADC with the DDC set to 0 Hz, channel 1 was driven by a 150 MHz IF input sine wave at 1 dBm from the Agilent E4400B generator. The code set the ADC to sample at 180 MHz. Thus the 150 MHz test tone was in the second Nyquist zone, and the undersampling folded the recorded samples down to $90 - (150 - 90) = 30$ MHz. The decimation factor was 2 for this experiment. A plot of this recording with the DDC enabled (but not downconverting) shows the sine wave sampled at 180 MHz in Figure 4.9. The DDC tuning frequency was set to 0 MHz, thus only real samples were generated and the Q samples were identically zero. Seeing that there were $90 \text{ MHz} / 30 \text{ MHz} = 3$ samples per cycle in the raw data output confirmed that the downconverted frequency was in fact a 30 MHz tone. Note that this is the Fourier transform of a real valued signal, which means that the magnitude spectrum should be symmetric about 0 Hz. Conjugate symmetry is a property of real signals, so this spectrum is in line with expectations.

The DDC's functionality was then tested by setting the tuning frequency to 55 MHz as motivated in Section 3.2.4. A 140 MHz test sinusoid generated by the DAC was used to drive ADC channel 1 – this was effectively a loop-back measurement to verify DDC operation. This was possible because waveform generation using `baseline_uct_demo` had been thoroughly tested. The DDC core generates an I/Q pair of each ADC sample. In this process there was a 2x decimation filter which resulted in a 90 MHz sample rate. The 140 MHz test tone folded down to 40 MHz. This was then downconverted by the DDC which was tuned to 55 MHz. The time domain recording and its Fourier transform are shown in Figure 4.10. The complex mixer tuned to 55 MHz translated this frequency down to a -15 MHz tone which has $90 \text{ MHz} / 15 \text{ MHz} = 6$ (complex) samples per cycle as expected. A spectral peak at -15 MHz is visible in the FFT. This signal is complex, so there is no expectation that its magnitude spectrum will be symmetric about 0 Hz. These results confirm that the down-conversion chain in the Cobalt is working with the frequency plan. The digitization of a swept frequency input would be tested by loop-back measurements, no additional configuration changes were required to digitize the $10 \mu\text{s}$, 50 MHz bandwidth LFM pulse used by the system.

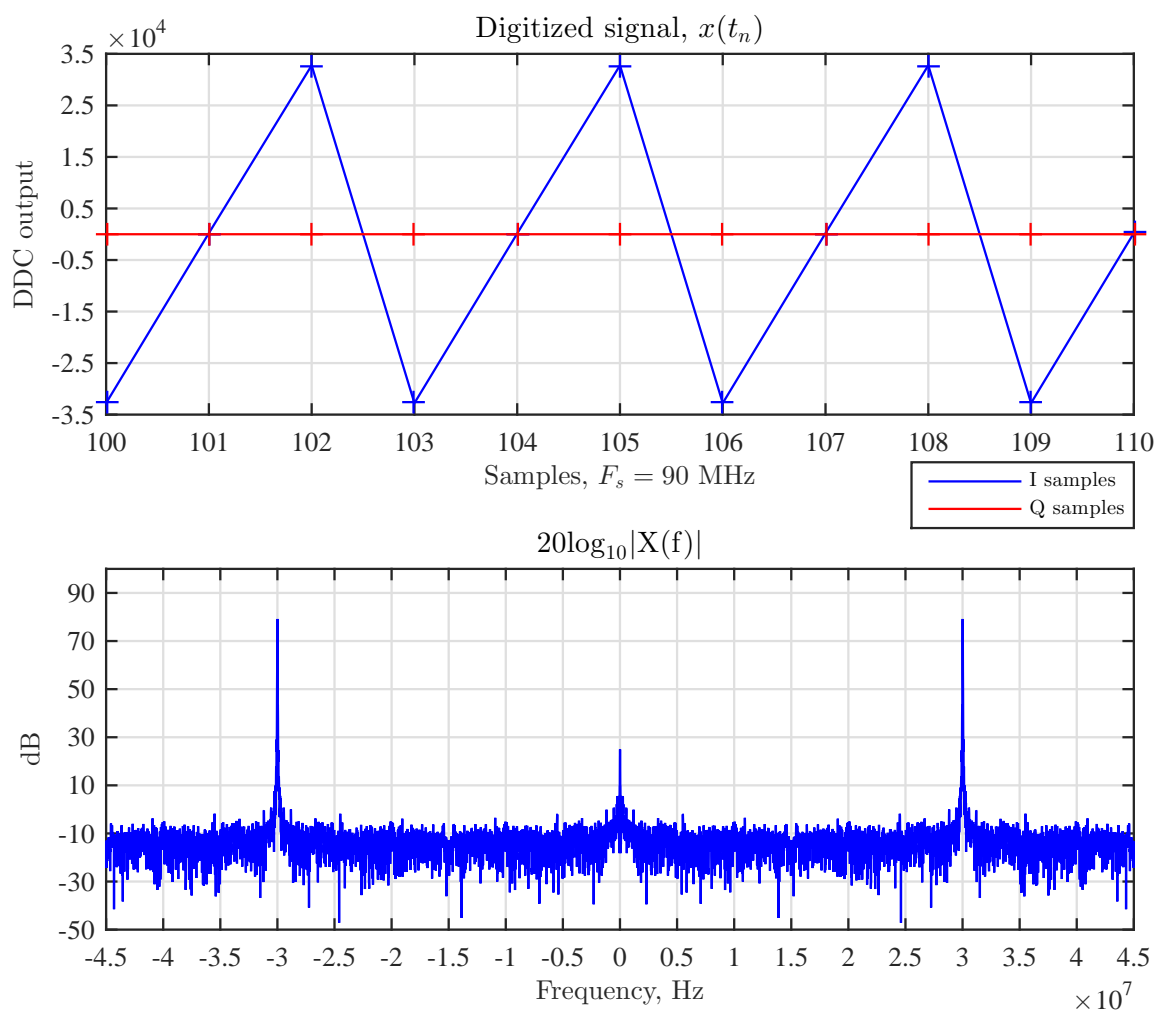


Figure 4.9: **Upper Plot:** Time domain samples $x(t)$ of digitized 150 MHz input signal from an Agilent E4400B ESG series generator undersampled at 180 MHz, resulting in a 30 MHz sine wave in raw samples. DDC tuning frequency 0 MHz, decimation 2x. Note that because the DDC NCO is set to 0 Hz, no phase shift is introduced to the waveform and the quadrature component is identically zero. **Lower Plot:** The log magnitude spectrum of the signal $x(t)$. DDC tuning frequency 0 Hz. Symmetrical spectral peaks at ± 30 MHz indicate real-valued DDC output.

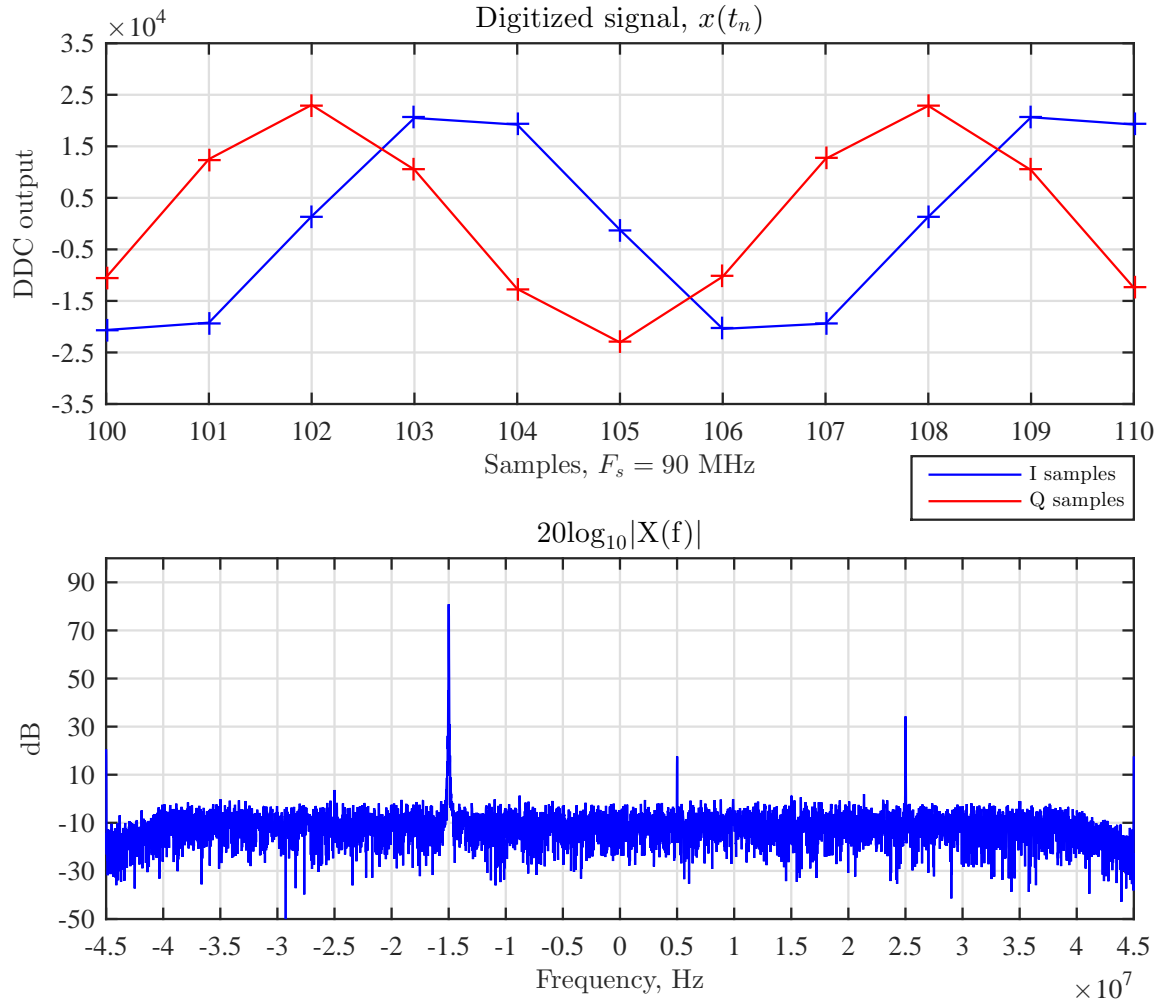


Figure 4.10: **Upper plot:** Downconverted time domain samples $x(t)$ of a digitized 140 MHz test tone generated by the DAC. A 15 MHz output is visible in the raw data, with six samples per cycle at 90 MHz confirming the frequency. The DDC decimation factor of 2x discards every other 180 MHz sample, resulting in a 90 MHz complex sample rate. Note that the complex multiplier in the DDC core generates a complex signal, which introduces a phase term.

Lower plot: The log magnitude spectrum of DDC signal $x(t)$. The DAC output frequency in this result was 360 MHz, with interpolation 2x. The peak at 25 MHz is due to the repeated spectral component at 220 MHz in the unfiltered DAC output being undersampled in the ADC's third Nyquist zone (from 180 to 270 MHz). This peak folds down to 140 MHz, then 30 MHz. The DDC 55 MHz tuning frequency then downconverts to $55 - 30 = 25$ MHz. Low-pass filtering the output of the DAC removes this unwanted component. The peak at 5 MHz has similar origin and can be removed by low pass filtering the DAC output.

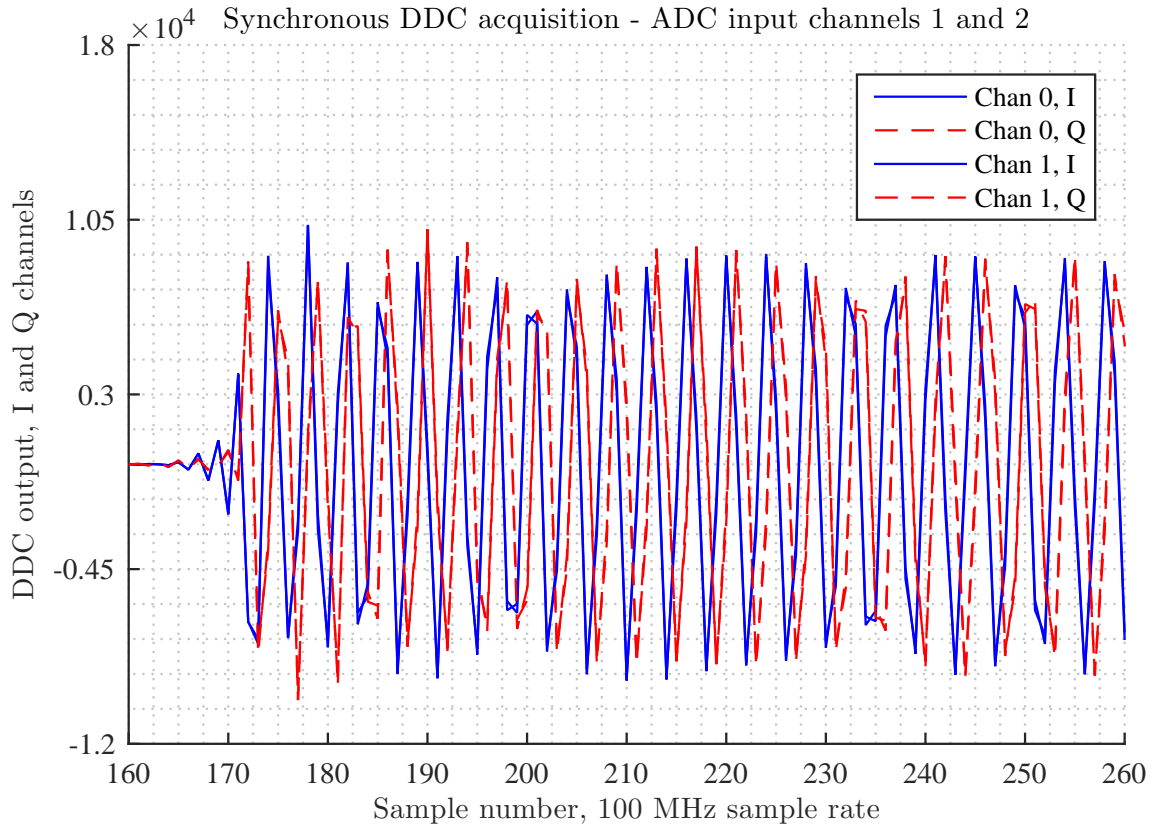


Figure 4.11: The DDC output from ADC channels 1 and 2. The signals driving the two input channels were identical sine waves. The ADC sample rate was 200 MHz and the decimation factor was 2, yielding complex sample rate 100 MHz. As is clear from the samples which coincide for both I and Q components, the DDC was able to synchronize its numerically controlled oscillator phases to zero on the trigger signal rising edge. The third channel, with identical setup in software, produced the same waveform.

4.2.2 Exp. B.ii: Synchronizing the DDC NCO on Trigger Events

To test the in-phase acquisition of multiple inputs, the modified version of `ddc_multichan` was used. This program enabled all three acquisition channels on the Cobalt board. The ADC was set to a 200 MHz sample rate with a 2x decimation factor. An input signal was supplied by a HP 4648D signal generator which also gave a 10 MHz reference clock to the AWG. A Mini-Circuits ZA3CS-400-3W-S splitter was used to fan out the sine wave and drive ADC channels 1 and 2. The AWG generated a trigger signal and synchronous 10 MHz clock to the Cobalt via its back panel connectors.

The controller program, `ddc_multichan`, opened the acquisition gate of each DDC channel using the external trigger signal, and the DDC numerically controlled oscillators were configured to reset on the same event. This ensured that the NCO phases on each DDC channel would be identical. The input sine wave was 70 MHz, and the DDC tuned to 40 MHz, downconverting to a 30 MHz sine wave at the input. The DDC output for this measurement is given in Figure 4.11.

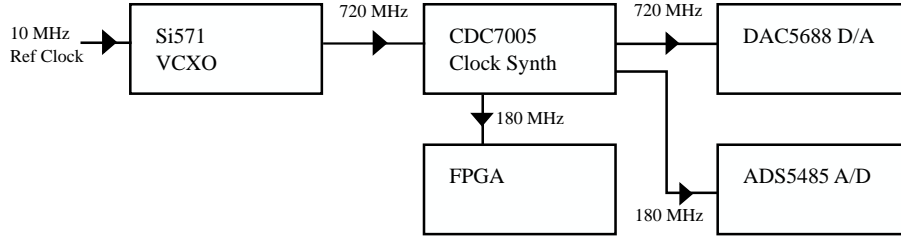


Figure 4.12: Clock distribution plan for NeXtRAD’s Cobalt-based digital transceiver. The timing and synchronization configurations for the DAC and ADC modules required different routing from what was used in the original `ddc_multichan` and `dac_trig` programs. The new strategy was to generate a primary 720 MHz clock (from the 10 MHz reference) in the CDC7005 which drove the DAC5688. Sub-multiples of this clock were then generated in the CDC7005 and distributed to the ADC modules and to the FPGA clocking domains servicing the transmit and receive signal paths.

4.3 Experiment C: Loop-back

The clocking scheme decided upon for the application is as depicted in Figure 4.12, see section 1.12 of [12] for details of clocking and synchronization in the Cobalt. The DAC clock is supplied by the CDC7005 clock synthesizer directly. Sub-multiples of this clock are then generated in the CDC7005 and supplied to the FPGA and the A/D modules. In the FPGA there are separate clocking domains for data paths servicing the A/D and D/A units, but both run at 180 MHz.

4.3.1 Exp. C.i: LFM Pulse Loop-back Autocorrelation

Computing the matched filter output of the loop-back recording of the LFM pulse and comparing it with the theoretical autocorrelation output gives a good indication that the signal processing chain is working. According to Skolnik et al [14], autocorrelation of an LFM pulse with time-bandwidth product $BT > 50$ can be well approximated by a sine-over-argument function:

$$\chi_{\mu}(\tau, 0) \approx |\text{Sa}(B\tau)| \quad (4.4)$$

where $\chi_{\mu}(\tau, f)$ is the radar pulse ambiguity function and the relative time delay τ is much less than the pulse length T , and $\text{Sa}(x) = \sin(x)/x$. The 3.01 dB time delay resolution $\Delta\tau$ is measured between values for τ for which

$$20\log_{10}|\text{Sa}(B\tau)| = -3.01 \text{ (dB)} \quad (4.5)$$

The time delay resolution can be determined directly from the autocorrelated recording of the LFM chirp using the above equation. The actual autocorrelation response resembles the product of a sinc

function and a triangle function, and when examined at time intervals much less than the pulse duration, the compressed response resembles a sinc function² very closely provided the time bandwidth product is larger than twenty according to Richards et al [19]. The sidelobes of compressed response of the 50 MHz, 10 μ s with a time bandwidth product of 500 will therefore have side lobe levels very near the usual -13.2 dB levels expected from a sinc function. It has been shown by Skolnik et al [14], that the compressed response of a 50 MHz LFM chirp has a 3.01 dB width of

$$\tau_3 = \frac{0.886}{B} = 17.7 \text{ ns} \quad (4.6)$$

Equations 4.5 and 4.6 generate the real and theoretical time resolutions. Taking into account the two-way range to a target, the standard 50 MHz LFM chirp would have range resolution

$$\Delta R_3 = \frac{\tau_3 c}{2} = \frac{0.886c}{2B} = 2.66 \text{ m} \quad (4.7)$$

where c is light speed. As an alternative to the 3 dB time width, the Rayleigh resolution could be used, which corresponds to the 4 dB time width, i.e. the time difference between the maximum signal level and the first null. The Rayleigh resolution is given by $\Delta R = \frac{c}{2B}$, which is exactly the same as Equation 4.7, but without the 0.886 factor. The 3 dB width is easier to measure than the Rayleigh width if a null is not easily distinguished in the compressed response of an LFM pulse.

To calculate the matched filter response, the loop-back recording of the standard NeXtRAD pulse was autocorrelated using a fast convolution approach, which is well documented by Richards et al [19]. The matched filter impulse response was generated from the recorded signal and was defined as follows

$$\mathbf{H} = \mathbf{S}^*, \quad (4.8)$$

where

$$\mathbf{S} = \begin{bmatrix} s[0] & s[1] & \dots & s[L-1] \end{bmatrix}^T \quad (4.9)$$

is the signal column vector form of the recorded signal of $L-1$ samples. It is well known that defining the matched filter in this way produces the greatest SNR value of the filter [19]. The discrete Fourier transform of both \mathbf{H} and \mathbf{S} are calculated using an implementation of the FFT to generate their frequency domain representations, $H[k]$ and $S[k]$ (k being the frequency index). \mathbf{S} was zero-padded to be about four times its original length to obtain smoother time domain output. The frequency domain matched filter output was generated by forming the product

²In this text, a sinc function refers to the sine-over-argument function: $\text{Sa}(t) = \sin(t)/t$

$$Y[k] = H[k] S[k] \quad (4.10)$$

By taking the inverse FFT of $Y[k]$, the discrete time output is produced:

$$y[n] = \text{DFT}_K^{-1} \{Y[k]\} \quad (4.11)$$

The log-magnitude of the calculated output $y[n]$ should match very closely the theoretical autocorrelation given by equation 4.5 for the 50 MHz bandwidth, 10 μs pulse. Any deviation would be minimal because any signal distortion introduced by the 2 m length of CNT100 cable routing the signal from the DAC to the ADC was negligible.

Loop-back Measurements

The autocorrelation response of the system was calculated from a loop-back measurement of the 50 MHz LFM pulse at the 125MHz IF. This was done using the experimental layout in 3.9, but without the low pass filter in the IF path. Both transmission and digitization were initiated by the 1 kHz external trigger signal supplied to the Cobalt module by an HP 33120A Arbitrary Waveform Generator, which served as the TCU. The program used to control the Cobalt was `baseline_uct_demo` with parameters as given in Table 3.2:

- DAC output interpolation rate 2x, output frequency 360 MHz,
- ADC sample rate of 180 MHz, DDC decimation factor of 2x, DDC tuning frequency set to 55 MHz.

The pulse used was the standard 50 MHz bandwidth, 125 MHz LFM pulse. The time domain representation of the waveform data loaded to RAM and the IF recording, both complex signals at base-band, are shown in Figure 4.13, and their corresponding spectra in Figure 4.14.

The autocorrelation of the IF measurements are shown in Figures 4.15 and 4.16. Clearly, the impulse response of the IF loop-back recording is consistent with the $\text{Sa}(t)$ expectation as

- the main lobe width is 17.76 ns, within 0.02 ns of the theoretical value in equation 4.6,
- sidelobe levels are 13.29 dB below the peak, within 0.09 dB of the nominal value $\text{Sa}(t)$.

This passes application test (C.i.) in Table 5.1. This measurement did not take into account the phase introduced by the NCOs in the up and downconverter chains of the Cobalt module, but naturally this had no impact on the magnitude output of autocorrelation calculation.

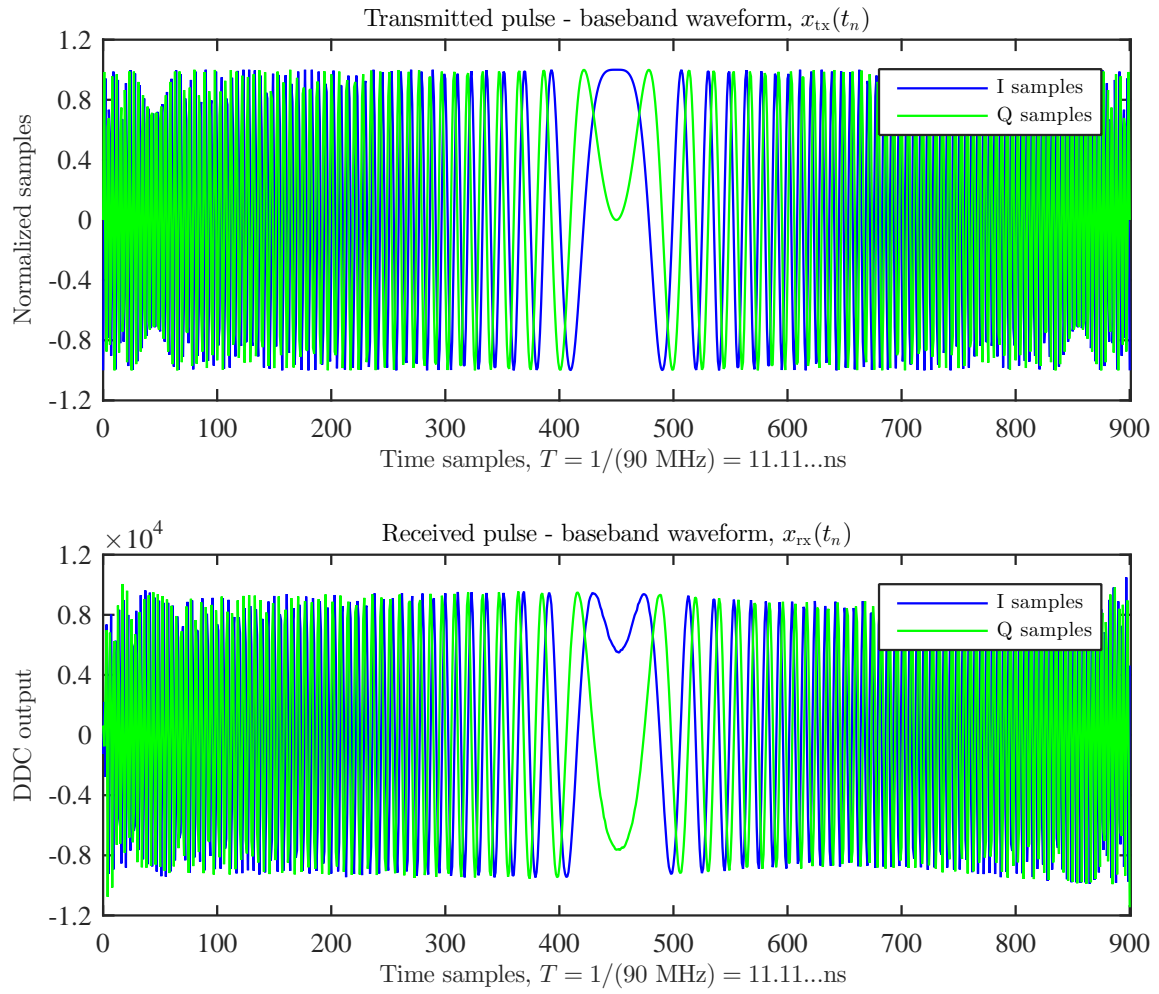


Figure 4.13: Loop-back time domain plots of transmitted data (upper plot) and received (lower plot) pulses at baseband. Clearly visible is the phase shift of the center frequency (0 Hz) component at the center of the pulse between the transmit and receive data.

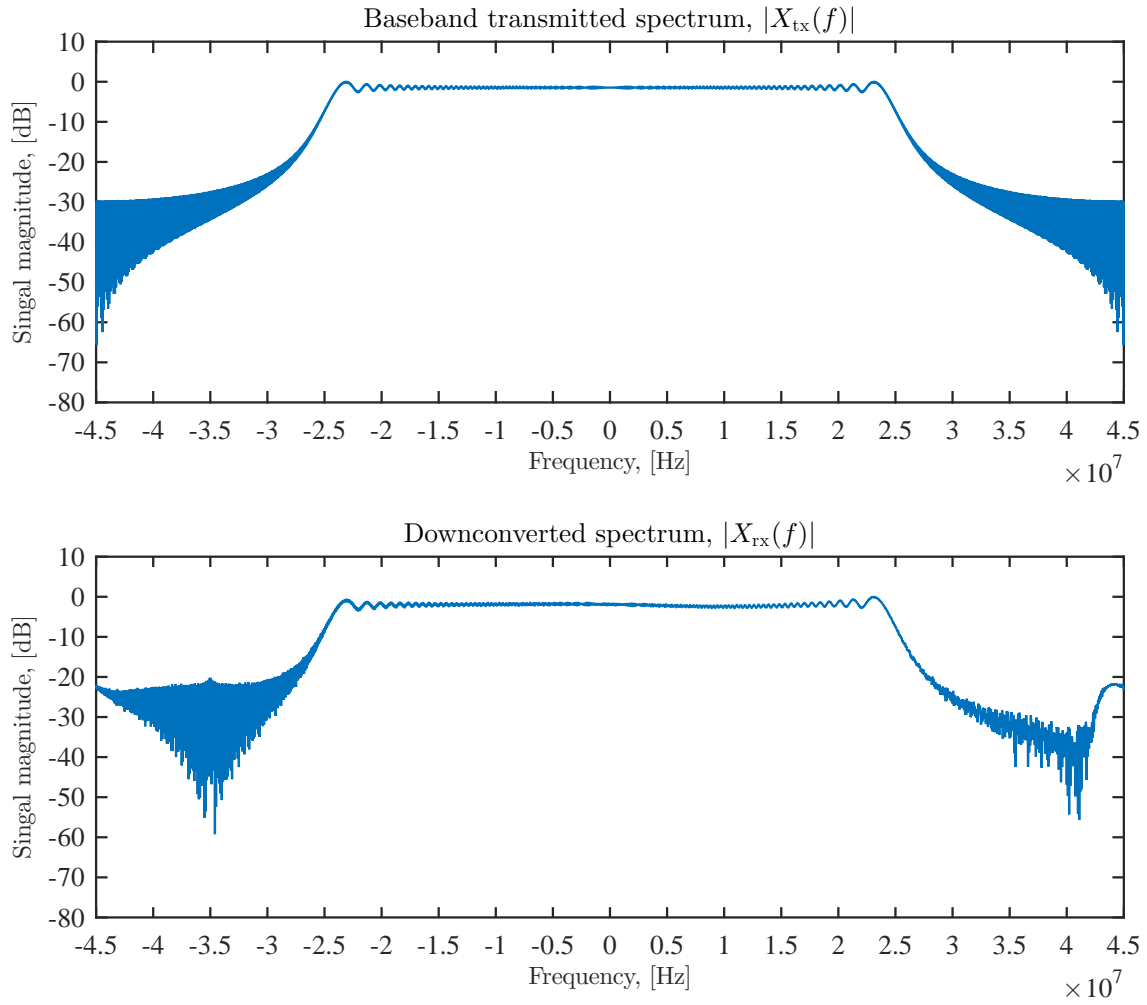


Figure 4.14: Normalized loop-back spectra of transmitted (upper plot) and received (lower plot) pulses at baseband. The 6 dB width of both plots is almost exactly 50 MHz as required by equation 4.3. This partially satisfies the objective of Experiment C.i.

Table 4.1: Pulse compression results for IF, X- and L-band Loop-back recordings. The 3 dB time width and corresponding range resolution are given for each test, with the height of the first sidelobe.

Frequency	$\Delta\tau_3$ (ns)	ΔR_3 (m)	Peak Sidelobe Level (dB)	Figure reference
IF	17.8	2.7	13.3	4.15 and 4.16
L-band	24.4	3.7	Not distinguishable	4.17
X-band	22.2	3.3	15.6	4.18

Loop-back measurements which included the REX were also taken to observe the effect this would have on the autocorrelation, but this was not part of meeting the user requirements. Figure 2.3 shows the signal configuration used to record the RF loop-back pulses, the only difference being that the RF output was routed directly back to the corresponding receive channel using a short, low loss coaxial cable. Filters in REX would introduce some group delay to the signal, so deviation from the theoretical $S_a(t)$ output was expected. These results are shown in Figures 4.17 and 4.18. The loop back recordings of the L- and X-band samples are in Appendix B. As can be seen in these impulse responses, there is significant broadening of the main lobe in the L-band autocorrelation, and nulls have been filled making it difficult to measure the sidelobe level. This is to be expected as the effect of the band pass filters in REX taper the pulse on both the transmit and receive channels. This tapering effect is less pronounced in the X-band pulse, as can be seen in the spectra of Appendix B. The tapering applied by the filters in the REX is roughly analogous to applying a window function to the pulse both on transmit and receive. Results of the IF, L- and X-band autocorrelations of loop-back measurements are summarized in Table 4.1.

4.3.2 Exp. C.ii: Loop-back to Constant Phase Value

A loop-back test in which a transmitted waveform was downconverted to a constant-phase complex value would indicate that the DDC and DUC were driven by clocks derived from one source. Such a measurement would indicate that multipliers were not introducing phase drift to the signal. This test was first done using `ddc_multichan` with settings slightly different from those given in Table 3.2:

- DAC output frequency of 200 MHz, DUC interpolation of 2x,
- ADC sample frequency of 200 MHz, DDC decimation of 2x, resulting in complex sample output at 100 MHz

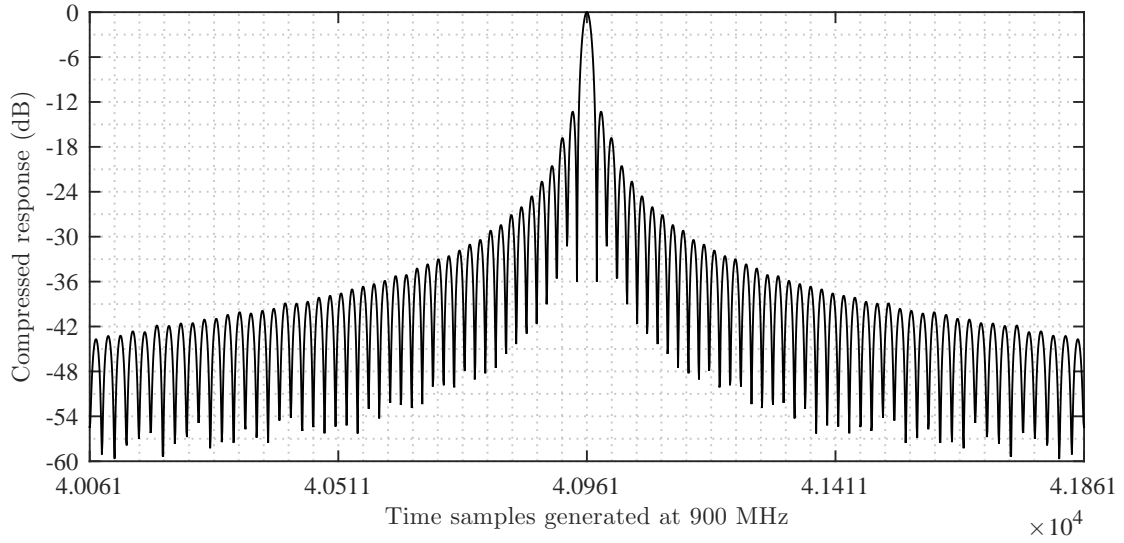


Figure 4.15: Autocorrelation of the intermediate frequency loop-back recording. This shows the time output of the compressed LFM pulse with a 50 MHz bandwidth. The high sample rate is a consequence of zero-padding the loop-back recording in Figure 4.13

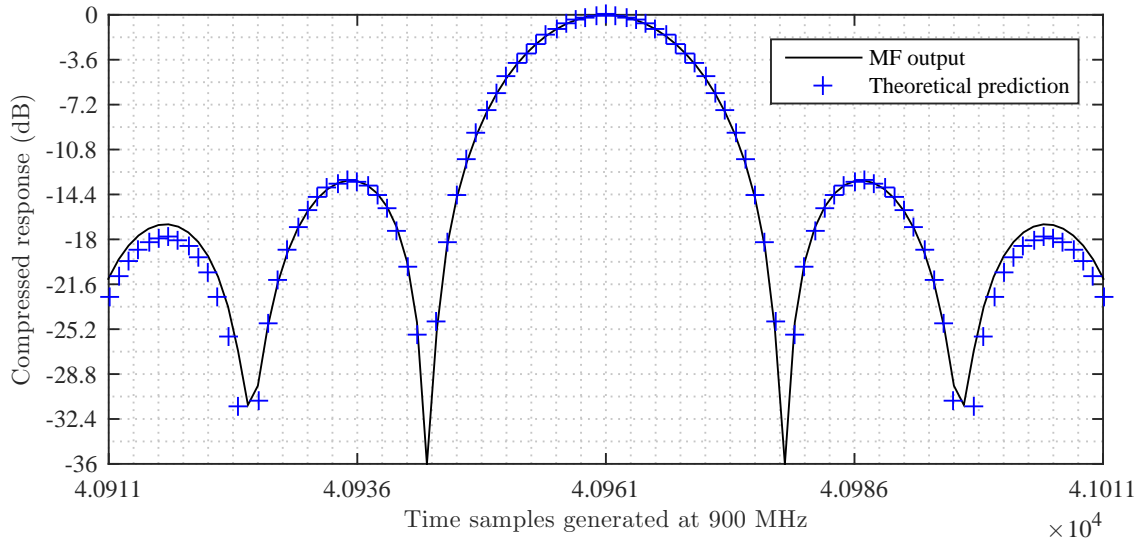


Figure 4.16: A zoomed view of the normalized compressed response of the 50 MHz LFM pulse in Figure 4.15. This shows the close agreement between the compressed response obtained from an IF loop-back measurement and the theoretically predicted $S_a(t)$ expectation. The -13.2 dB sidelobes and 3 dB width match almost perfectly. However, for time values further away from the peak, the approximation deteriorates as is visible from the second sidelobe(s).

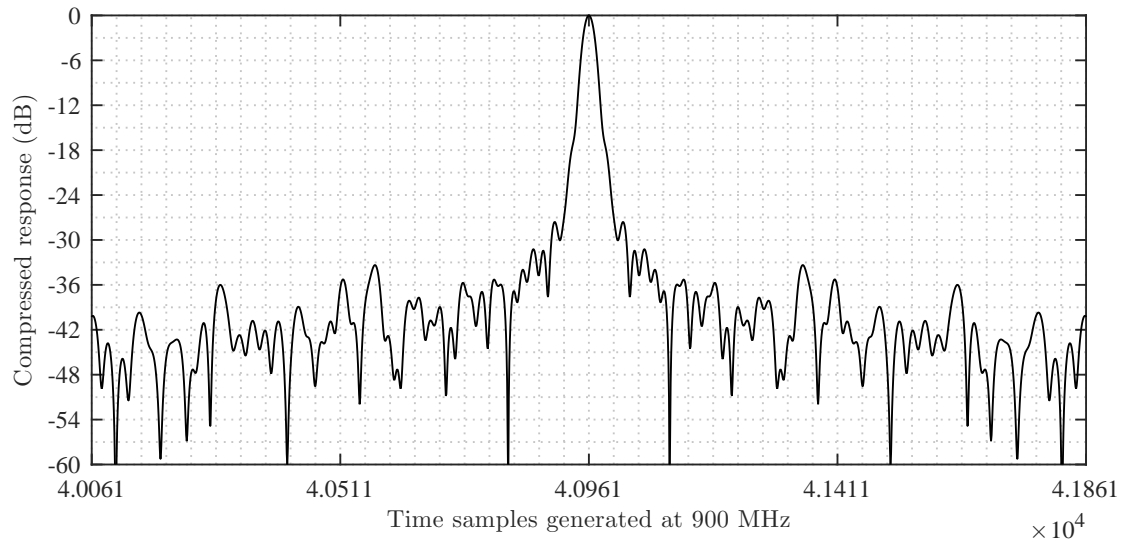


Figure 4.17: L-band loop-back compressed response for a 50 MHz LFM chirp. The first null has been filled due to signal distortion in the signal path, but the mainlobes appear to be lower as might be expected after windowing. There is also an increase in the breadth of the mainlobe.

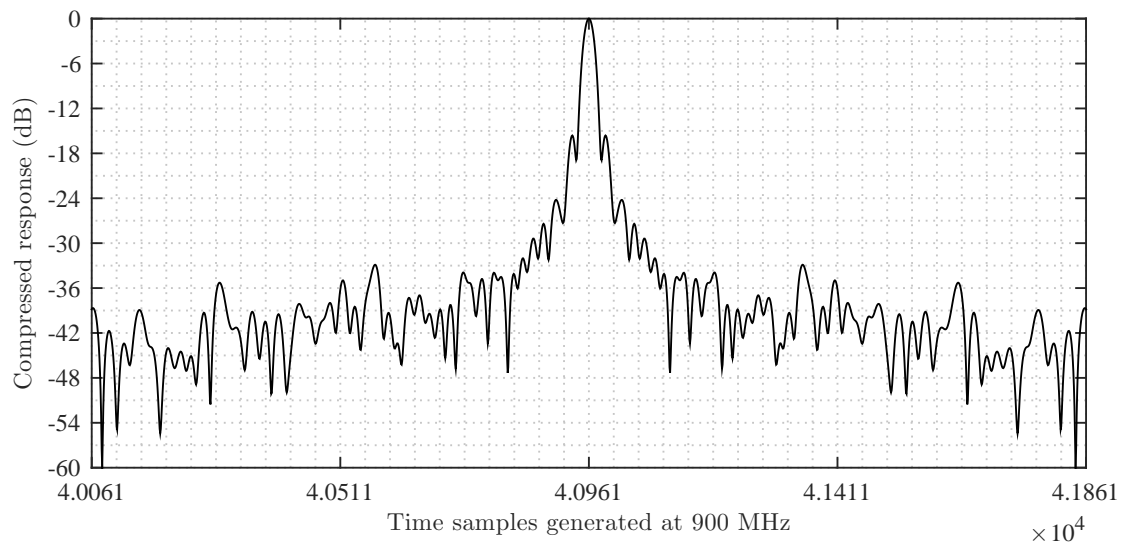


Figure 4.18: The X-band compressed response for the standard 50 MHz pulse. The first nulls and sidelobe peaks are visible in this plot, now reduced to about -16 dBm. The 3 dB width of the main lobe is slightly broader than that of the IF pulse compression in Figure 4.15.

The ADC and DAC sample frequencies were set equal to make debugging easier. Test sine wave of 6.25 MHz was generated in the code, which is reduced to 3.125 MHz with the DAC interpolation set to 2. The DUC tuning frequency was 75 MHz. The 6.25 MHz tone was upconverted to $75 - 3.125 = 71.875$ MHz. To set the DDC tuning frequency 71.875 MHz would therefore down-convert the transmitted tone to a constant complex “DC” value. It was believed that phase of the DC value would be dependent on $T_{\text{delay_DAC}}$, jitter in this output delay had been observed in waveform generation experiments (see Section 4.1). After several repeated measurements it was apparent that there were two distinct phase values obtained corresponding to two values for $T_{\text{delay_DAC}}$, which differed by 5 ns. Plots DDC raw data for these two phase positions and their corresponding phase are shown in Figure 4.19. These plots show that position A had a zero-valued Q component corresponding to zero phase, but position B had a phase offset of roughly 132° . The ADC only starts acquiring samples at around the 300th clock cycle. All three DDC channels produced identical values for a given phase position. The variation in phase seen in position A and B could have been caused by either variation in $T_{\text{delay_DAC}}$ or in variation in the ADC acquisition delay, $T_{\text{delay_ADC}}$. The task of measuring $T_{\text{delay_ADC}}$ was difficult as a perfect digitizer was not available to compare the actual ADC recording to. However, DAC output jitter dependence on the upconverter interpolation rate had been observed in earlier experiments. Therefore, it was strongly suspected that the DAC output jitter, and not the ADC, was the source of phase uncertainty between runs in loop-back measurements as seen in Figure 4.19.

It was observed in earlier experiments that the output delay of the DAC would vary by a clock cycle between runs, measured to be $\Delta T_{\text{delay_DAC}} = 5$ ns on the oscilloscope. Once the DAC had started transmitting, $\Delta T_{\text{delay_DAC}}$ would have a constant value for the duration of the measurement. The variation happened between measurements and produced a phase difference in the recorded waveforms, as is clear from the plots in Figure 4.2. This phase corresponds neatly to phase position B in figure 4.19. A 200 MHz clock cycle delay of the DAC output waveform with frequency $F_{\text{wave}} = 71.875$ MHz would produce roughly a 130° phase offset, viz:

$$\Delta\phi = 2\pi \Delta T_{\text{delay_DAC}} F_{\text{wave}} = 129.375^\circ \quad (4.12)$$

The source of $\Delta T_{\text{delay_DAC}}$ could have been introduced by the multiplier in the digital upconverter. However, IP cores which implement the receive and transmit data paths are in separate clocking domains on the FPGA. This led us to suspect that the clocking domains were not perfectly synchronous. To investigate this possibility, the Gate B signal responsible for internally triggering the digital upconverter on the DAC5688 ASIC was delayed using Sync Bus Input Delay Tap Control Register designed for this purpose [21]. Input delays of up to 2.325 ns could be programmed in 75 ps increments for any of the gate or sync signals in the Cobalt’s clocking circuitry. Delays of 0, 1.125 and 2.325 ns were introduced to the DAC trigger signal whilst leaving the ADC trigger signal undelayed. If mismatch

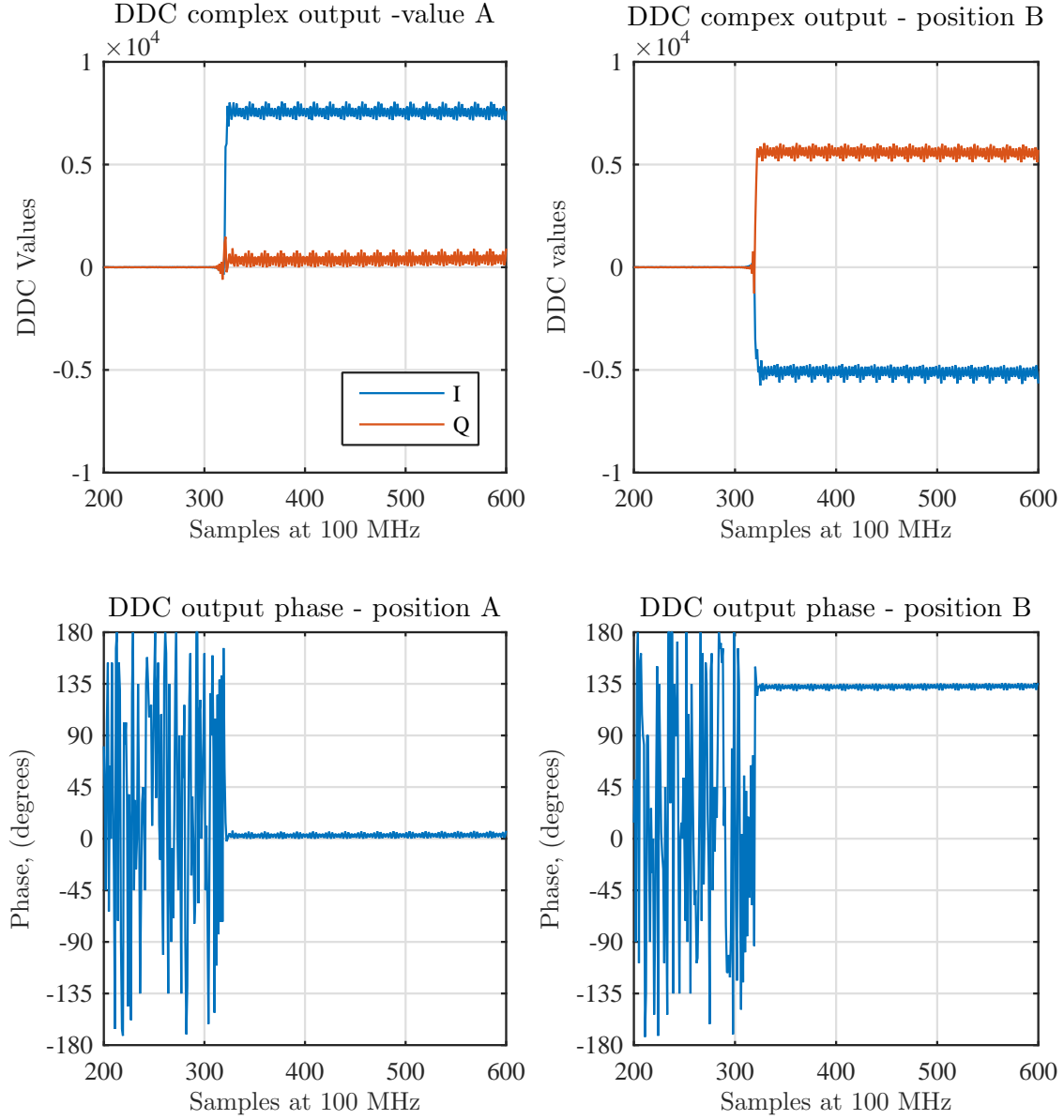


Figure 4.19: DDC complex data and phase of position A (left column) and B (right column) of the loop-back to DC experiment from a single downconverter channel. Position A corresponds to a DAC output delay of $T_{\text{delay_DAC}}$, and position B to a delay of $T_{\text{delay_DAC}} + 5$ ns. The 5 ns (one 200 MHz clock cycle) delay corresponds roughly to a 132° phase shift of the downconverted input waveform. Waveform data arrives at the DDC at sample number 320, phase of the noise in earlier samples is random (lower plots).

between the clocking domains was a problem, the delay introduced the DAC clocking domain should have been sufficient to result in predictable behaviour from run to run. However, none of the delays produced any change in the amount of run-to-run jitter observed in the DAC output, which remained at 5 ns. The apparent < 280 ps pulse-to-pulse variation in $T_{\text{delay_DAC}}$ on the oscilloscope was probably much smaller in reality (on the order of a few tens of picoseconds), and therefore negligible.

Whether the output delay was $T_{\text{delay_DAC}}$ or $T_{\text{delay_DAC}} + 5$ ns, it would not prevent successful doppler processing, provided it was constant during a measurement. The 5 ns variation could have been caused by a FIFO reset in the DAC5688 ASIC during initialization, but it was more likely because of clock outputs of the CDC7005 clock synthesizer not quite lining up the same way between initializations. The final controller program, `ddc_multichan`, used a 4x interpolation rate to reach the 720 MHz DAC output frequency, and the ADC decimation factor was 2x as with previous versions of the controller. In principle, this small change should not produce any additional uncertainty in the output delay of the DAC between consecutive outputs. If there were a jitter problem in a multi-pulse loop-back measurement, it would manifest as large phase jumps in a single range bin from pulse to pulse.

To determine the phase stability of the system over a longer period a 1 kHz, 10 s loop-back recording of an L-band pulse was done using the finalized version of `ddc_multichan`. The transmitted LFM pulse was of $0.5 \mu\text{s}$ duration with a 50 MHz bandwidth and the ADC recorded 512 samples at 90 MHz. The trigger signal was produced by an AWG. A 200 m long coaxial RF cable routed the REX L-band output to the L-band input. The compressed response of each pulse was then calculated, producing a time-domain response similar to that in Figure 4.17. The phase of the peak compressed response for each output was $-88.651 \pm 0.359^\circ$ (sample mean \pm sample variance). The phase values ranged from -90.058° to -87.324° . The phase is plotted in Figure 4.20.

Coherent integration of N recorded pulses will increase the SNR by a factor of N . As has been shown by Richards [20], the SNR improvement is

$$\chi_N = \chi_1 \quad (4.13)$$

The linear relationship between the number of pulses coherently integrated and the peak SNR value of the compressed response was demonstrated for 10 000 pulse L-band recording in Figure 4.21.

4.4 Experiment D: Transmit and Acquisition Control

After the frequency scheme was tested and working correctly the timing of signal generation and digitization could be optimally configured. The code for doing this was developed in preparation for the first RF tests. Experimental parameters that would impact the digital transceiver setup included:

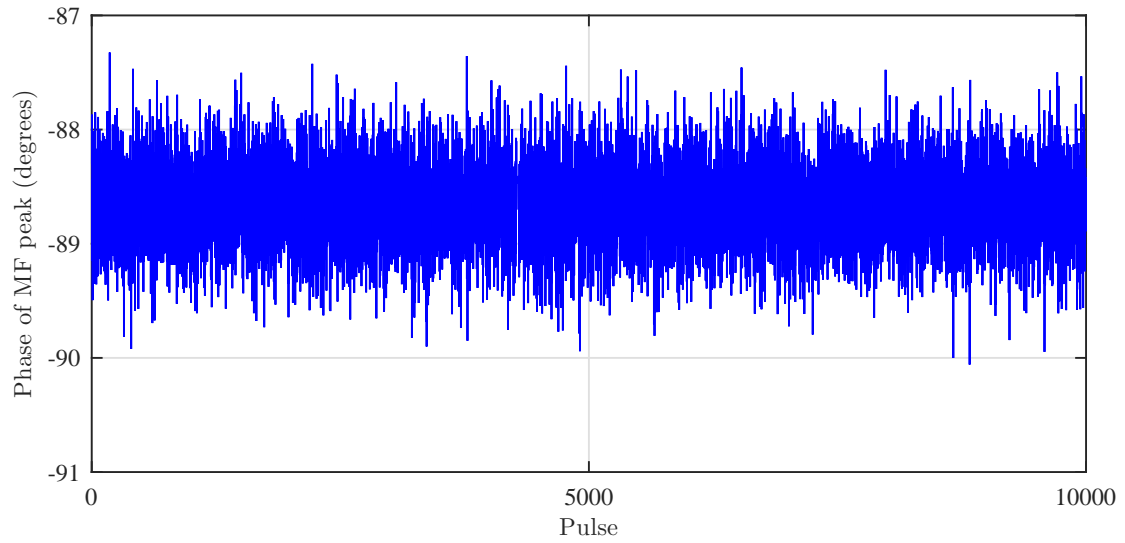


Figure 4.20: Compressed response peak phase of a 10 000 pulse L-band recording. The phase value is $-88.651 \pm 0.359^\circ$, and the values range from -90.058° to -87.324° . The pulse duration was $0.5 \mu\text{s}$ and bandwidth 50 MHz.

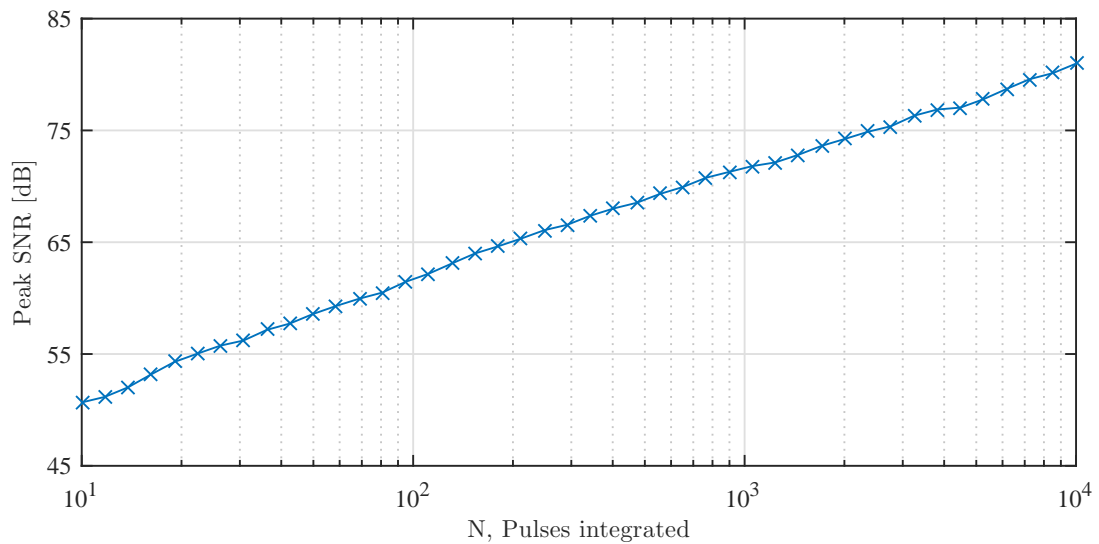


Figure 4.21: Peak SNR vs number of pulses integrated for the 10 000 pulse recording at L-band. This graph shows that the SNR increases by a decade per decade increase in pulses integrated, as required by Equation 4.13.

- Maximum range and blind ranges which would determine the recording length and the transmit pulse durations respectively.
- The number of different pulse durations to be stored in the DAC RAM. This would affect the number of complex samples to be supplied to the DAC.
- Delays in transmitting or digitizing, which could be set in terms of ADC or DAC clock cycles.

The Readyflow library supplied with the Cobalt included a linked list data structures for controlling waveform generation, digitization, and direct memory access (DMA) channels. This was done by configuring linked list elements in the `baseline_doppler_demo` C program for the DUC and DDC channels. These same linked list elements were subsequently used for the final `ddc_multichan` with some minor alterations to account for differences in sampling and interpolation rates.

The timing diagram for NeXtRAD's digital transceiver system is shown in Figure 4.22, which shows timing structure from the Cobalt module's perspective for three pulses. Note that the timing control unit will generate additional trigger signals, not depicted here for the high power amplifiers. Two axes represent fast and slow time. The first PRI is represented by the axis in the foreground and starts at 0 PRI, at the rising edge of the external trigger signal. This activates the DUC and DDC linked lists in the Cobalt module. The DAC linked list is programmed to wait for $T_{\text{DAC_delay}}$ DAC clock cycles ($f_{\text{DAC}} = 360$ MHz) before transmitting the waveform. The $10\ \mu\text{s}$ chirp is generated over $N_{\text{chirp}} = \tau f_s = 3600$ samples, after this the DAC output is disabled.

The ADC and DAC linked lists operate independently. After the initiating trigger pulse at $t_{\text{slow}} = 0$, the ADC is programmed to wait long enough for the first echo signals of interest to return, which are just beyond the blind range of the radar. This requires $0.25T_{\text{DAC_delay}} + N_{\text{chirp}}$ of the DDC clock cycles ($f_{\text{DDC}} = 90$ MHz). After the delay the ADC starts digitizing. The number of samples to digitize is given by

$$M = \frac{2(R_{\text{max}} - R_{\text{min}})}{c} f_{\text{DDC}} \text{ [samples]} \quad (4.14)$$

where the maximum range is R_{max} , the blind range is R_{min} , and c is light speed. After recording the ADC is deactivated, linked list pointers are reset awaits the next trigger event.

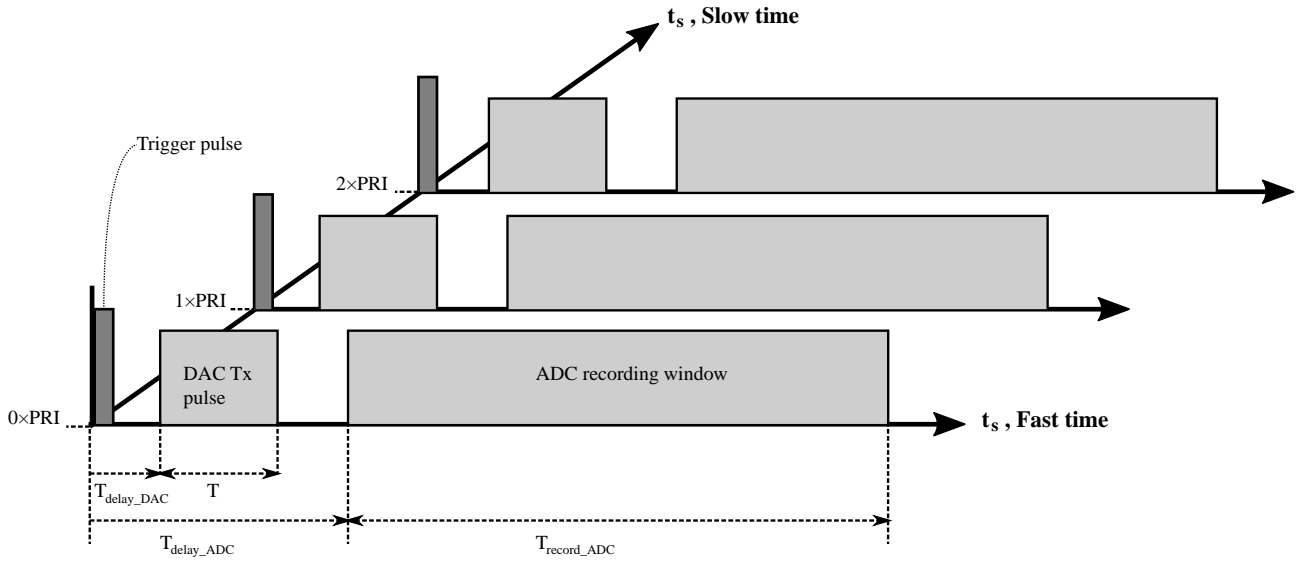


Figure 4.22: A timing diagram showing the fast and slow time axes. Each PRI is triggered by the arrival of a rising edge on the external trigger input from the timing control unit. After the initial trigger, A programmable delay of $T_{\text{delay_DAC}}$ precedes the generation of the transmit pulse by the DAC, which has duration T . After the same trigger event, the ADC acquisition is delayed for a programmable duration $T_{\text{delay_ADC}}$ which is completely independent of the DAC delay. After this, it digitizes a predetermined number of samples in a time period of $T_{\text{record_ADC}}$. This process is repeated at a rate equal to the PRF until the required number of cycles have elapsed. Note that this is from the digital transceiver perspective – more elaborate timing schemes are required for the RF front end of NeXtRAD.

4.4.1 Linked List Setup

A typical measurement the active node will transmit and record for 180 s at 1 kHz PRF. For each transmitted pulse there is a precise sequence of operations that the DAC and DDC must execute. The same applies for the ADC and DDC. Detailed instructions for configuring the linked list engines for the ADC and DAC are given in sections 3.2 and 3.3 of [12] respectively.³ The linked lists enable complex gating for transmission and recording. When setting up these elements it was important to know the sample frequencies of the DUC and DDC outputs, as timing is specified in terms of these clock rates. The details in this section are the minimum required to configure the linked list engines for transmitting and recording.

The DAC5688 chip has an output sample frequency 360 MHz. The DUC generates samples at $f_{s_DUC} = 360$ MHz. In a typical experiment the DAC operates as follows:

1. On the first three trigger events transmit nothing. This facilitates noise recording.
2. On the fourth trigger transmit the waveform. Active gate period X clock cycles.

³Future users are urged to consult these documents as slight deviation from correct setup will result in either improper transmission or digitization of waveform data.

3. Repeat step 2 $N + 3$ times, generating a total of N pulses.

The ADC samples at 180 MHz and operates concurrently with the DAC. With 2x decimation the DDC generates baseband samples at a frequency of $f_{s_DDC} = 90$ MHz - a quarter of DUC sample rate. It executes the following sequence of operations:

1. Wait for 3 ADC clock cycles. This N -sample delay can be adjusted to match the blind range of the radar.
2. Acquire 6000 data samples on ADC channel 1. At a 90 MHz sample rate this corresponds to a 10 Km range.
3. Repeat $N + 3$ times.

DAC Linked List

These DAC instructions are translated into a 4-element linked list with elements initialized to values in table 4.2. Each linked list element in the table has the following variables (see section 3.3 of the Pentek Model 71620 Operating Manual):

Delay The delay before the DAC begins to generate an analogue signal. It is set in terms of DAC clock cycles and has a minimum value of 1. In the first three links it is set equal to twice the recording length of the ADC (still much shorter than the PRI) to ensure nothing is transmitted so that only noise is recorded. The function of this delay is to allow the digital upconverter NCO to settle after synchronization. If this is not done, the transients caused by the synchronization of the NCOs will be transmitted, which is undesirable. This delay value can be set to any value between 1 and 2^{32} .

Gate length This controls the number of samples the DAC will remain active. This is set to 1 (the minimum valid setting) in linked list elements 0 through 2. Note that this is not what prevents transmission during the first few PRI cycles, that is done by setting the Delay variable.

Repeat The waveform will be generated for a total of (repeat) times each time the linked list element is executed. This is always set to 1. The DAC output channel is disabled by the controller program after the maximum number of transmit pulses have been reached.

RAM offset Transmit waveforms are pre-loaded onto the Cobalt DDR3 SDRAM. This parameter specifies the start address of given waveform. The DAC output controller reads bursts of eight 32-bit samples per address, which dictates that this variable must be a multiple of eight, minus one (e.g. 7, 15, 23). If this condition is not met, the waveform data will not be correctly read from RAM.

RAM length This is the number of 32-bit RAM memory positions to load starting from the RAM offset address. In combination, the offset and length variables can be used to access any contiguous block in RAM. As with RAM offset, this variable must also be a multiple of eight, minus one.

Next link The link to execute when the next trigger event happens. In this setup the linked list hops through the first three elements and then repeats the fourth indefinitely, or until the controller program exits.

It was possible to select any portion of a waveform loaded into RAM using the RAM offset and RAM length parameters described above. In this implementation, a waveform table consisting of baseband LFM chirps with different durations was generated. The controller program then loaded this file into the Cobalt RAM and accessed portions of it as directed by the linked list output control engine. To access each waveform, the RAM offset and length variables for each predetermined waveform were hard-coded into the controller program, and the waveform index was supplied by the experiment header file.

ADC Linked List

The ADC linked list is much simpler than the DAC's. It consists only one element, as is shown in Table 4.3. The significant parameters in this list are:

Gate length Specifies the recording window length in terms of 16-bit ADC samples. Note that a consecutive pair of 16-bit samples acquired by the ADC at 180 MHz translates to a 32-bit word generated at 90 MHz when the DDC core is running at 2x decimation. With these settings, gate length variable equals the number of 32-bit complex samples generated by the DDC.

Repeat As for the DAC linked list this is always set to 1.

Next link There is only one element in this linked list, so this is always set to element 0.

4.4.2 Acquisition Result

Using the linked list structures, the a loop-back recording of several pulses using `ddc_multichan` was made, the result is shown in Figure 4.23. The data was captured using a loop-back measurement of a $1\ \mu\text{s}$ pulse. The configuration of the number of pulses to transmit and the waveform to select were read from a text file by the `ddc_multichan` executable during the measurement. This demonstrates both transmit and acquisition control of the data, satisfying user requirements 8, 9, and 11. In addition, this particular measurement accepted parameters from a text file, which satisfies user requirement 12.

Table 4.2: DAC output control engine linked list parameters. These can be reconfigured to suit different transmit requirements.

Link Definition	Element	Dec/Bin	Hex
0	Delay	48000	0xBB80
	Gate Length	6000	0x1770
	Repeat	1	0x1
	RAM offset	0	0x0
	RAM length	1	0x1
	Wait for trigger? 0 = yes	0	0x0
	Next link	1	0x1
1	Next link	2	0x2
	<i>Other parameters are the same as link 0</i>		
2	Next link	3	0x3
	<i>Other parameters are the same as link 0</i>		
3	Delay	1	0x1
	Gate Length	5407	0x151F
	Repeat	N-1	0xN-1
	RAM offset	0	0x0
	RAM length	5407	0x151F
	Wait for trigger? 0 = yes	0	0x0
	Next link	3	0x3

Table 4.3: DDC control engine linked list parameters.

Link Definition	Element	Dec/Bin	Hex
0	Delay	1	0x1
	Gate length	6000	0x1770
	Repeat	1	0x1
	Wait for trigger? 0 = yes	0	0x0
	Next link	0	0x0

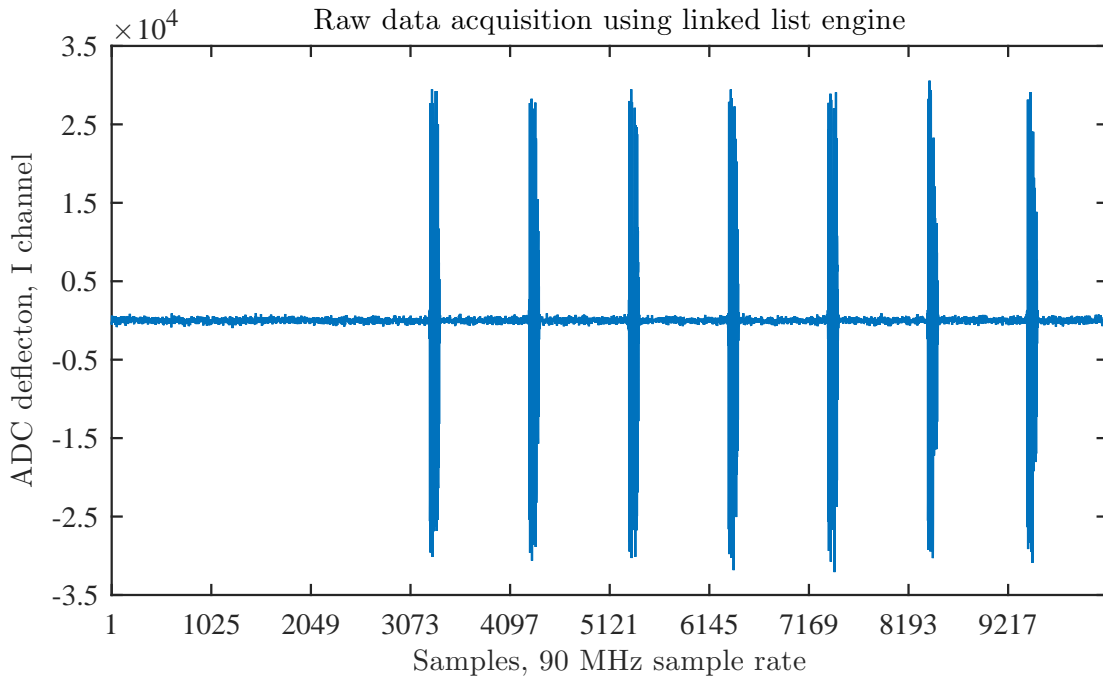


Figure 4.23: This plot shows 10 PRIs worth of data recorded by ADC channel 1, each consisting of 1024 complex samples, in an RF loop-back measurement. The transmit and acquisition control linked list engines were configured as per Tables 4.2 and 4.3, except for differences in the DDC recording length, and DAC RAM offset and length variables. The first three PRI blocks record only noise, and afterwards a $1\ \mu\text{s}$ pulse was transmitted in each of the seven remaining pulses. This plot shows that the operation of both the transmit and digitization channels can be precisely controlled using the linked list engines.

4.5 Experiment E: PRF Test

The maximum PRF at which the digital transceiver can operate depends on the rate at which the system can move data from Cobalt RAM to system memory via the PCIe bus. Multi-channel acquisition will reduce the maximum PRF. This is because of data transfer from each of the three ADC channels is handled by three threads which compete for system resources until all the channel data is written to disk via the PCIe interface.

Memory Requirements and Data Rates

Each DDC-generated complex sample requires 32 bits (four bytes) of data to store. Using equation 4.14 the number of bits stored per PRI is therefore $32M$, where M is the number of 32-bit DDC samples stored. A recording of T_{rec} s will require

$$D = 32MT_{\text{rec}} \text{ PRF [bits]} \quad (4.15)$$

In a typical measurement will have parameters $T_{\text{rec}} = 180$ s at a PRF of 1 kHz, with $R_{\text{max}} = 10$ km and $R_{\text{min}} = 1.5$ km. This will require about 5100 samples per pulse, and 19.9219 KiB⁴ per second of data. Equation 4.15 predicts that 3.67 GB per receive channel will be needed to store the data.

Multichannel Acquisition

The original multichannel acquisition `ddc_multichan` code engaged all three A/D modules and their corresponding digital downconverter IP cores. Each of the three DDC cores on the FPGA stream data from an ADC FIFO engine, see section 1.7, *Digital Down Converter (DDC) Core*, of [21]. The `ddc_multichan` program instantiates one thread per DMA channel to handle data transfers from the ADCs to disk storage on the host computer. Acquisition is triggered by an external trigger event and ends after the required number of samples (which usually correspond to the DMA data buffer size) has been stored. After that, each FIFO generates an interrupt which starts data transfer to disk via the DMA channel. Once all the DMA channels have completed their transfers (which could be in any order), the system is ready for the next transfer. If the external trigger rate (the radar PRF) is too high, triggers may occur before the DMA transfers complete. This usually results in the program crashing. To prevent crashes the following factors must be taken into account:

- The PRF and buffer size. Larger data buffers take longer to write to disk, increasing the risk of program crashes.

⁴1 kibibyte = 1024 bytes.

- It is important that the system uses a dedicated PCIe bus for the Cobalt module. High-performance graphics cards will compete for system resources with a Cobalt module using a PCIe interface.
- By using fewer ADC channels, or at least preventing file writes in one or two of the DMA threads, the amount of data and the number of times memory needs to be accessed can be reduced. This allows the digital transceiver and host computer slightly more time to complete data transfers between trigger events.

Maximum PRF Results

The maximum achievable PRF would depend almost entirely on the host computer's capabilities. The maximum PRF was explored using two different host computers. Loop-back experiments were done at Pentek to get an idea of what the highest PRF would be. Acquiring data from all three DDC channels the highest stable PRF was 2.5 kHz. This was with each channel acquiring 16384, 32-bit complex samples per pulse, more than three times the required size for a 10 km range with a 10 μ s pulse. This was done for several hundred of pulses without data loss. The specifications of the computer used to do this recording were as follows:

Operating System: Ubuntu 12.04 (64-bit)

Hard Drive: Seagate Barracuda 7200.10, 220 GB

Processor: Intel Core i7-3820, 3.60 GHz, 8 cores

RAM: DDR3, 1600 MHz, 16 GB

The Cobalt host computer at UCT used an Intel i7 processor, 8GB RAM and a 120 GB solid state hard drive (SSD). SSDs typically have significantly higher IOPS (input/output operations per second) figures than disk drives. It is therefore reasonable to expect that much higher PRF's will be attainable with the UCT system. The data from each channel is stored in a corresponding file, to which the recording of each range bin is appended. Using all three DDC channels as developed in the final Cobalt controller program `ddc_multichan` it was possible to record 1024-complex samples per channel per pulse, at rates exceeding 4 kHz. The Pentek machine was able to cope with over 16 000 samples per pulse with all DDCs active at 2.5 kHz. Given that no more than two channels will need to be recorded simultaneously in any given pulse in the final system, and that the SSD used in the UCT machine was faster than the disk-based drive, the final system will easily cope with two record channels at a 2 kHz PRF. This will satisfy the user requirement for multichannel acquisition at a high PRF.



Figure 4.24: Configuration A, showing the Reutech printed dipole array antennas supported by a timber frame, Tx above and Rx below. These were used for the first low-power, single-pulse measurements.

4.6 Low Power Monostatic Prototype Measurements

The low-powered prototype was constructed to test the performance of the digital transceiver in a simple monostatic radar setting. These results were not intended to test the system against specific user requirements, rather they provide confirmation that the system is able to collect radar data for range-doppler analysis. The range vs. pulse compressed output graphs presented in this section were the result of several measurements taken from the George Menzies Building roof, which is utilized for many similar radio frequency experiments. Precise details of the equipment used in test configurations A through D are given in Table 3.3 and Figure 3.10. Photographs of these antenna configurations are shown in Figures 4.24, 4.25, 4.26, and 4.27. The primary target for many of these measurements is shown in Figure 4.28.

The earliest test results were obtained using configuration A, which used the printed dipole array antennas for transmit and receive, as shown in Figure 4.24. A $1\ \mu\text{s}$ pulse was used to take single-pulse measurements of the PD Hahn Building. The match-filtered output in Figure 4.29 showed peaks corresponding to the range of large scatterers the line of sight, including the Library, Career Services, and PD Hahn buildings at ranges of 145, 190, and 250 m respectively. Note that the reference pulse used to produce these graphs was obtained by doing an RF loop-back measurement of the transmit pulse, which excluded the effect of antennas on the signal. The same measurement of the PD Hahn building using Configuration B produced similar peaks to the original single pulse measurements,



Figure 4.25: Configuration B for L-band measurements, which used Poynting Direct A-LPDA-0020-V2, which are 680-2900 MHz broadband antenna with a 60° beamwidth in elevation and azimuth. The antennas are mounted on a SkyWatcher tripod, in vertical polarization orientation.



Figure 4.26: Configuration C for L-band measurements, which used a sectoral horn antenna for receive (on the left) and a reflector dish antenna for transmit (on the right). The PD Hahn building 270 m away is clearly visible against the horizon, just behind the steel post.



Figure 4.27: Configuration D for X-band measurements. The X-band horn antennas had a 3 dB beamwidth of 10° , in elevation and azimuth.



Figure 4.28: Target scenery of the Upper Campus of the University of Cape Town, used for low-powered measurements of the PD Hahn building. 10° , 20° and 60° beamwidths are shown in to give an indication of what was visible to the radar in each of the antenna configuration tested. Also shown is the parking lot area which was used to take doppler measurements.

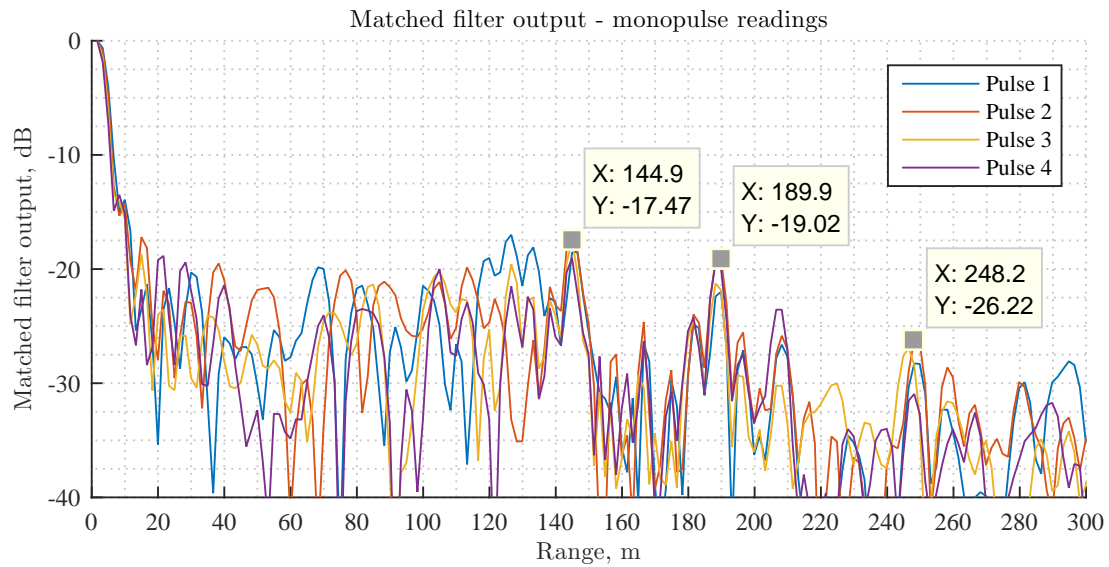


Figure 4.29: Figure of the matched filtered pulses obtained with configuration A L-band measurements, using the Reutech printed dipole array antennas. Although the antennas had a narrow azimuth beamwidth, the elevation beamwidth was greater than 60° , which meant that many targets in the line of sight were illuminated by the transmit pulse in addition to the PD Hahn building. This accounts for the several additional peaks at ranges less than 250 m. A peak created by reflections from the library building are visible at approximately 145 m. Zero range in this plot corresponds to the autocorrelation peak of the transmitted pulse. Pulse length was $1 \mu\text{s}$.

as can be seen in Figure 4.30. The Poynting Direct antennas of this configuration were not very directional with their enormous 60° azimuth and elevation beamwidths, so there was a considerable amount of clutter in the matched filter output when targeting PD Hahn.

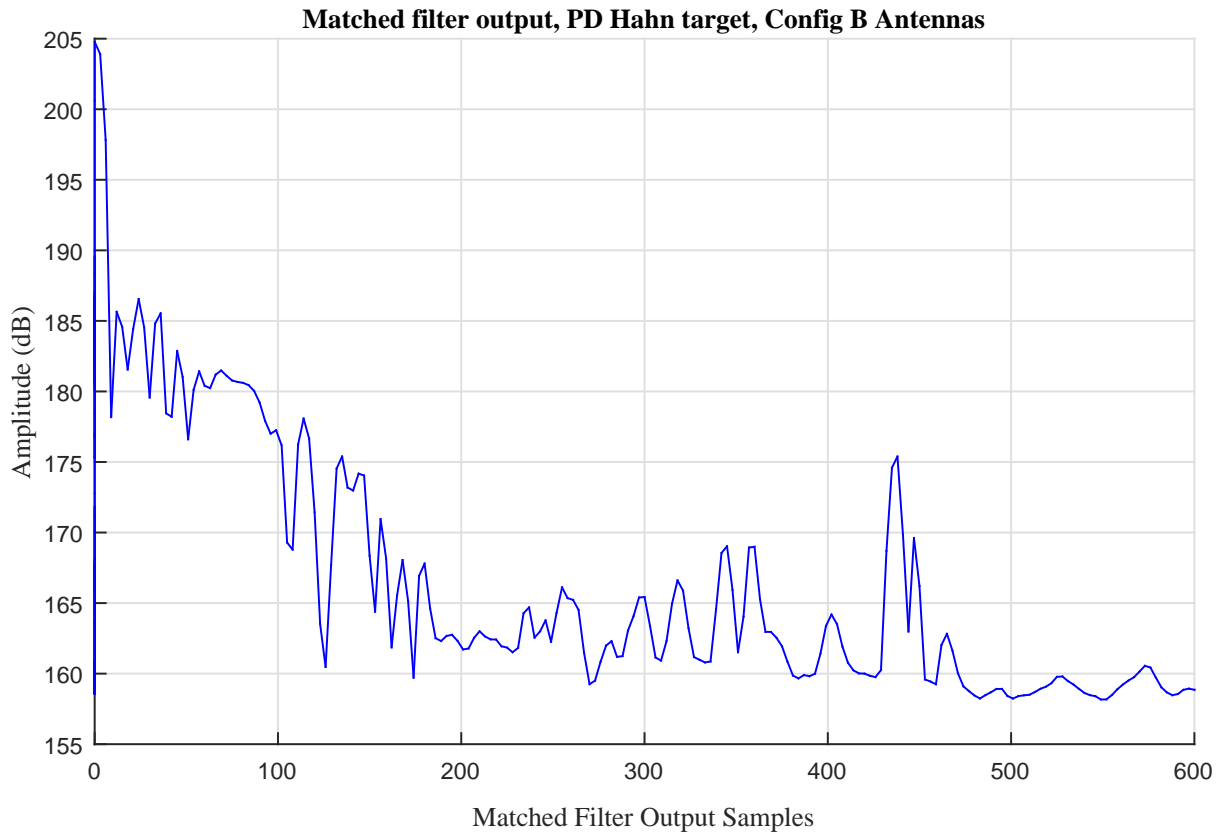


Figure 4.30: Matched filter output obtained using Configuration B antennas. Matched filter output has not been scaled. The pulse length used was $0.6 \mu\text{s}$. Sample 0 corresponds to the correlation peak of the transmit pulse with the reference. Acknowledgment: Dr Matt Ritchie, UCL, who processed this data.

Configurations C and D were also tested and produced measurements of the PD Hahn building quite similar to what was obtained in Figures 4.29 and 4.30, however, the signal levels at the peaks were different. These could be due to differences in the antenna gains, and also because different buildings may have been illuminated in spite of efforts to keep the antennas aimed at the same target. It was notable that with the 10° beamwidth X-band antennas of configuration D, the PD Hahn building could be aimed at quite accurately, producing a far more pronounced peak in the matched filter output than was previously obtained with the other configurations, as can be seen in Figure 4.31.

The more interesting measurements using the L- and X-band configurations C and D are shown in Figures 4.32 and 4.33. These figures show the doppler shift of a human target moving toward and away from the transmitting antenna. These measurements were taken at a 1 kHz PRF using a $0.6 \mu\text{s}$ pulse. The target scene was a nearby parking lot, which visible from same vantage point the other measurements were taken from (see Figure 4.28). The moving target was the author, who moved toward and away from the roof-top transmitter along a 15 m path for a minute during each measurement. The L-band measurement of this motion was taken with configuration C, and the doppler vs

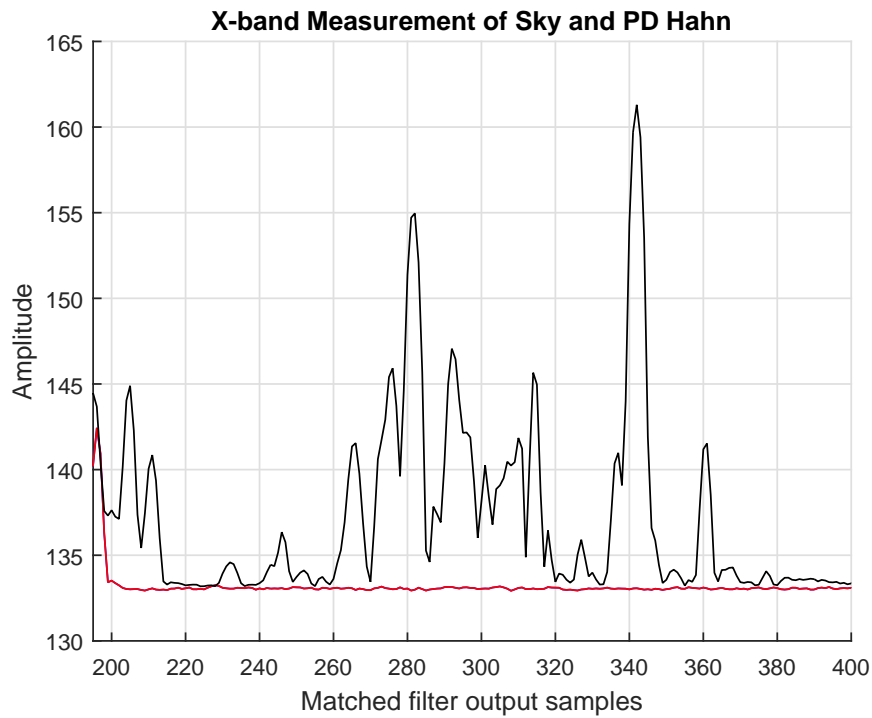


Figure 4.31: X-band measurement of the PD Hahn building (black) and sky (red). With 10° beamwidth in azimuth and elevation, the PD Hahn building produced a very pronounced peak at sample 340 in the matched filtered data using a $1\ \mu\text{s}$ pulse. Pointing the antennas up at the sky produced no return signals at all, as can be seen from the red trace. Note that the sample axis has not been scaled. Acknowledgment: Dr M Ritchie of University College London, and Dr F Fioranelli, University of Glasgow, who processed this data.

time graph generated from the recording is shown in Figure 4.32. Approximate target velocity can be determined from this time-doppler plot by using the familiar equation relating doppler shift and carrier frequency [19]:

$$v = \frac{c f_d}{2 f_c}$$

where v is radial velocity, f_c is the carrier frequency, c is the speed of light, and f_d is the doppler shift. For the L-band recordings, the doppler shift was $f_d = 35$ Hz at $t = 5$ s, and the carrier frequency $f_c = 1.3$ GHz, which translates to $v = 4.0$ m/s. This is roughly running speed. The X-band measurement data produced the data shown in Figure 4.33. The target produced a $f_d = +100$ Hz doppler shift at the $f_c = +8.5$ GHz, or $v = 1.7$ m/s radial velocity toward the transmitter which is a brisk walking speed. Also visible in this graph is a strong doppler return from about 12 to 22 s with a +25 Hz doppler shift. This was a car which reversed out of a parking space during the measurement. At $t = 30$ s, the car accelerated away from the transmitter and out of the target area. It is evident that the car presented a much larger radar cross section than the author, returning a 10 dB stronger signal level in Figure 4.33. Visible in both of these plots is a strong signal with zero doppler shift. The fact that the 0 Hz peak remained at 0 Hz and that the moving human target produced realistic doppler shifts indicated that the digital transceiver was not introducing random phase shifts to the transmitted and recorded waveforms.

4.7 Summary of Application Test Procedure Results

Experiment A in Section 4.1 concerned waveform generation. The aim was to generate phase-stable, low-jitter waveforms. Both phase and jitter could be measured using an oscilloscope provided that its acquisition was initiated by the same external trigger signal that drove the waveform generation from the DAC. Figure 4.1, which shows 68.75 MHz sine wave being generated by the DAC5688 I-output channel.

Without supplying both the arbitrary waveform generator and the Cobalt with a 10 MHz reference signal, the jitter between the trigger and the DAC output appeared to be over 12.5 ns on the oscilloscope display. By supplying the reference signal to both the AWG and Cobalt, whilst still triggering the scope acquisition with from the AWG, the output jitter subsided to about 3.2 ns. This was only an approximate indication of the actual output jitter, because the jitter between the AWG internal oscillators and the Cobalt's internally generated clock could be quite large in spite of a common 10 MHz reference. This showed DAC output delay was difficult to measure without a precise view of the internal trigger signal. To supply this internal signal, the Cobalt board was configured to generate an LVPECL signal in response to the external trigger and this was used instead to trigger the oscilloscope acquisition. The result captured by oscilloscope, given in Figure 4.2, showed that the DAC

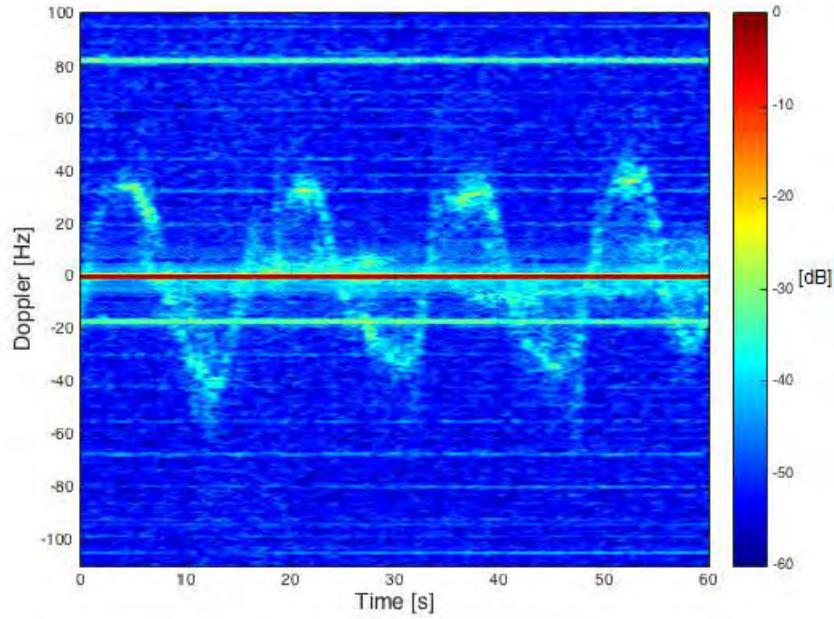


Figure 4.32: L-band micro-doppler measurement of a pedestrian target running toward and away from the transmitter, taken with antenna configuration C. The colour scale corresponds to signal level in dB. The constant frequency signals at -18 Hz and +82 Hz are possibly due to communications signals collected by the receiver. Acknowledgment: Dr M Ritchie of University College London, and Dr F Fioranelli, University of Glasgow, who processed this data.

output waveform was remarkably stable with a constant phase when generating the output waveform at a 1.25 kHz PRF. Clearly, the numerically controlled oscillator was generating a constant phase offset to the generated waveform and the output jitter was below 280 ps with respect to the internal trigger signal.

The full 50 MHz LFM chirp spectrum at the 125 MHz IF was generated with DAC output frequencies of 360 MHz using 2x interpolation, and at 720 MHz using 4x interpolation. These output spectra are visible in Figures 4.6 and 4.7. These results verify that the upconversion frequency plan in Section 3.2.3 was successfully implemented. The user requirements for waveform generation of the LFM chirp were met by these ATPs.

Digitization tests in Experiment B (Section 4.2) showed that the digital downconverter core was operating as expected. This was tested by supplying the A/D input channels with sine waves of known frequency and digitizing these inputs. Using an NCO frequency of 0 Hz showed that the undersampling of an 150 MHz input signal at 180 MHz did indeed produce a I-valued tone at 30 MHz. This is shown in Figure 4.9. To test the down-conversion functionality of the DDC IP core, a very simple loop-back measurement was done by supplying a 140 MHz input signal to the ADC from the unfiltered DAC output. This was only possible because the DAC output was properly configured in Experiment A. Tuning the DDC NCO frequency to 55 MHz produced the expected -15 MHz tone in

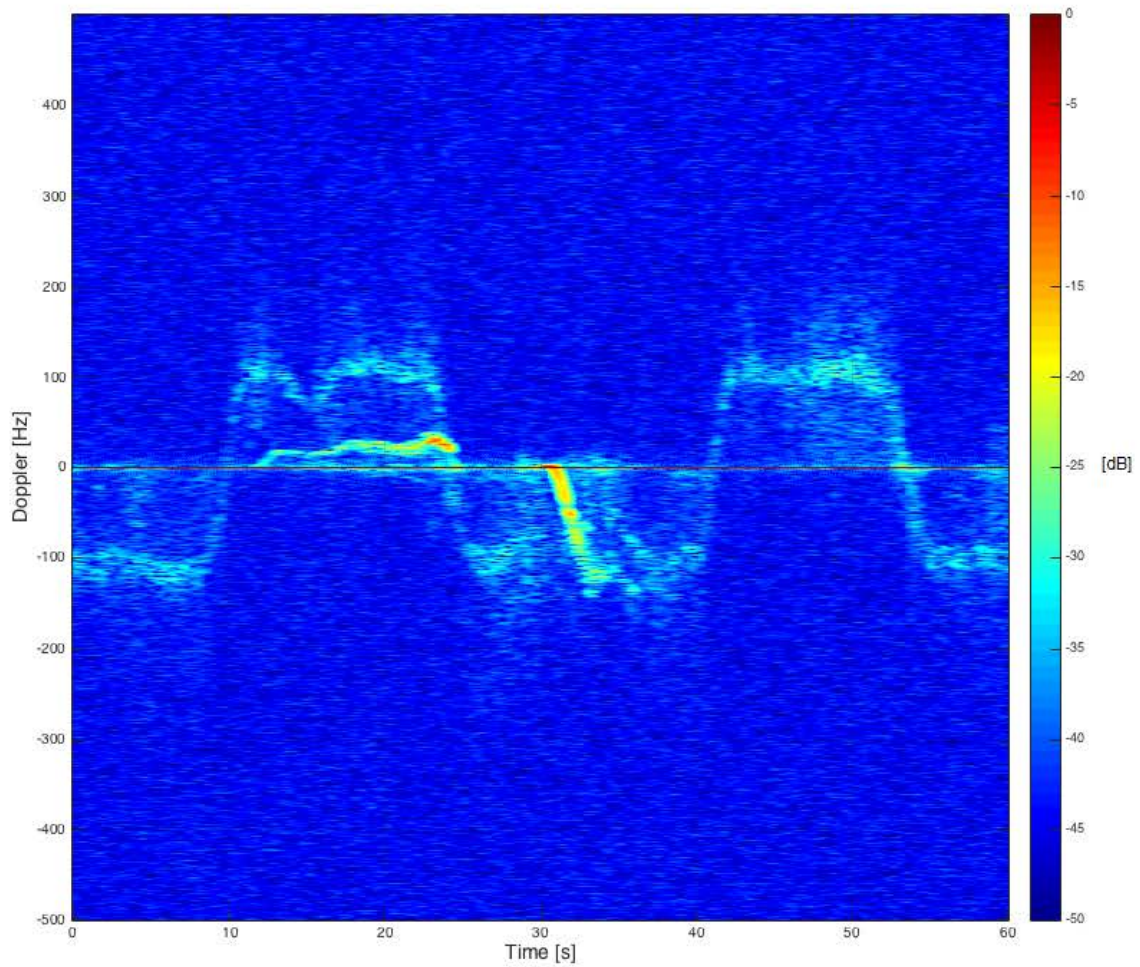


Figure 4.33: Configuration D, X-band doppler measurement showing a doppler plot of the same pedestrian target walking toward and away from the transmitter repeatedly over a 60 second period. Also visible are strong return levels from a car which moved out of a parking space during the measurement. Acknowledgment: Dr M Ritchie of University College London, and Dr F Fioranelli, University of Glasgow, who processed this data.

the analytic signal as shown in Figure 4.10.

It was also shown that the digital downconverter's numerically controlled oscillators were resetting to zero phase at the external trigger event. This was analogous to the DAC NCO resets configured in Experiment A (Section 4.1). Phase resets were demonstrated for two of the input channels in Figure 4.11. Thus, experiment B met the user requirements for phase coherent multichannel digitization. Digitization of the full spectrum was to be tested in Experiment C, where the phase stability of both up and down-conversion channels would be simultaneously tested.

Loop-back measurements using the full 50 MHz bandwidth LFM pulse were used to calculate the compressed response of the waveform, as in Experiment C.i. (Section 4.3). Plots of the generated and downconverted loop-back data and their corresponding spectra are shown in Figures 4.13 and 4.14. The compressed response of this LFM pulse exhibited the characteristic $Sa(t)$ form around the peak, as can be seen in Figure 4.16.

Experiment C.ii. was designed to measure overall system jitter. A loop-back measurement in which a generated sine wave was downconverted to a zero-frequency term showed that there was transmit delay variation equivalent to about one clock cycle in the DAC5688 output waveform. This can be seen by the two different phases in Figure 4.19. After the board is initialized, the DAC output delay remained constant, so this uncertainty will not affect Doppler-processing of recorded data. In any measurement, the total jitter contributed by the Digital transceiver is below 500ps, satisfying user requirement for low jitter contribution from this system.

Linked-list engines control the operation of the Cobalt's transmit and recording operation. These lists were configured as per the user requirements, and tested in Experiment D (Section 4.4). These settings were used for every subsequent measurement and proved reliable in testing of the low powered prototype system. An example of a loop-back recording which used the transmit and digitization linked-list controllers is visible in Figure 4.23.

Experiment E tested the maximum PRF the system was capable of. It was discovered that the digital transceiver would operate reliably at a PRF of 2 kHz, and that higher stable operating frequencies were possible. The maximum PRF depended heavily on the maximum rate at which the system under test could write to access system memory. Using a solid state hard drive greatly increased the rate at which data could be written to memory. The access times of individual writes will affect the maximum PRF, therefore the more receive channels are active, the more time will be required to store data recorded in a PRI. The number of recording channels used and samples digitized per pulse, per PRI, will also affect the maximum PRF achievable.

Simple testing was used to get an indication of the digital transceiver's maximum achievable PRF rather than a thorough analysis of the data rates and memory access latencies of the two systems tested. A maximum PRF of 2.5kHz was achieved with over 16 384 samples per pulse, three channel-recording using a disk hard drive. Using the faster solid state hard drive of the final NeXtRAD system

and comparable resources for processing and RAM, the final system will easily meet and exceed the 2 kHz PRF requirement for single and dual channel recordings.

The final version of the digital transceiver controller program included a parser which would extract measurement parameters from an experiment header file, to satisfy user requirement 12. The variables included the number of pulses to transmit and digitize, and the number of samples to delay ADC acquisition. This capability was incorporated into the final controller program which was used in the low power measurements. One example of the parsing capability of the final controller program, `ddc_multichan`, is shown in Figure 4.23. More complex transmit and acquisition patterns are possible with the linked list engines, but the result obtained from Experiment F was sufficient to meet the fundamental control requirement.

The results from the low-powered test radar served as additional confirmation of the digital transceiver's suitability for its role. The system was relatively easily integrated with its neighbouring subsystems in a prototype radar system, in particular the REX. These measurements used a variety of antenna systems and low power amplifiers. The PD Hahn building was detected using four different antenna configurations. The highlight of the measurements were the detection of moving vehicles and pedestrian traffic by their doppler shifts. Phase-stability and low-jitter operation of the system, so carefully arranged in the ATP experiments, enabled these measurements.

Chapter 5

Conclusion

The digital transceiver has been shown to meet the user requirements by successful completion of application test procedures as summarized in Table 5.1. These tests have demonstrated that the board is able to transmit and digitize 50 MHz bandwidth signals at a 125 MHz intermediate frequency, with phase stability and minimal jitter as shown in Sections 4.1, 4.2 and 4.3. It was demonstrated that the system could produce phase-stable, pulse compressed output over a 10 s loop-back recording at 1 kHz, and coherent integration was demonstrated by the linear increase in the SNR as a function of pulses integrated, Figures 4.20, 4.21 in Section 4.3. The digital transceiver was able to perform its signal processing operations at a pulse repetition frequency of over 2 kHz (Section 4.5). The system was able to synchronize its internal oscillators to an external 10 MHz reference clock and accept a trigger pulse which initiated its operations for each cycle, and could interchange signals with the receiver exciter to be used in the final active node of the radar.

The development of control software for the Cobalt module was the key to successfully completing application test procedures contrived to ensure compliance with the user requirements. Although versatile, the Cobalt module is difficult for non-initiates to configure for bespoke signal processing tasks. To overcome these hurdles required an appreciable level of assistance from product specialists at Pentek, in addition to several months of testing and development in the UCT microwave laboratory. After an intensive three-week product support visit to the Pentek laboratories in New Jersey, USA, the signal processing and coding challenges were finally mastered, opening the gateway to phase-coherent, multi-channel operation from the Cobalt module.

To serve as confirmation of the suitability of the Cobalt module for the digital transceiver role in NeXtRAD, short range radar measurements of static and moving targets were taken from the roof of the George Menzies building at UCT campus (Section 4.6). Analyzing the recorded data revealed that static and moving targets were in fact detectable. Most importantly, useful doppler information confirmed the phase stability of successive pulses. The digital processing operations in these tests are very similar to what will be required in the final system. It can therefore be concluded that work done

in this project can now be readily applied in further development of the NeXtRAD system.

5.1 Recommendations for Further Work

5.1.1 Amplitude Weighting of Transmit Pulses

Correction of frequency distortion in REX would increase the total energy of the transmitted pulse. In Appendix B, it can be seen that the spectrum of the output of the REX is not of uniform amplitude across either output RF band. This is due to filters and amplifiers in the transmit chain of REX, and it reduces the energy of the transmitted pulse. Similar distortion is likely to be present on the down-conversion chain. Correcting these distortions will result in some improvement of the signal to noise ratio in the compressed response. It is possible to apply amplitude weighting to the baseband transmit pulse in software, which would result in a level amplitude at the RF output of REX. The weighting would need to be matched to the amplitude distortion of each of the three output channels of REX. However, to accomplish this it will be necessary to amplify the DAC intermediate frequency output signal level as REX requires an input between 3-7 dBm. The maximum output of the Cobalt DAC unit is approximately 2.7 dBm, which REX can accept, but it is not ideal. Applying this weighting function will sacrifice some of the DAC dynamic range, but this could be outweighed by the gain in SNR.

5.1.2 Full Exploitation of Waveform Generation Capability

In the low power testing several transmit pulses were generated and loaded into the Cobalt RAM before each experiment. These pulses were all 50MHz LFM chirp pulses with lengths ranging from 0.6 to 10 μ s. There is 1 GB of DDR3 SDRAM available on the 71621 Cobalt module, enough to store more than ten thousand different waveforms of 10 μ s length with complex samples generated at 180 MHz. The useful bandwidth of the transmit chain in the DAC is about 70 MHz, and there may be room for slightly more bandwidth in the REX transmit and receive chains to exploit. Unexploited capability exists to transmit a very wide range of different waveforms from RAM using the lined list output control engine. The possible applications of a more versatile waveform generator include symbiotic and cognitive radars.

5.1.3 Use of Software Debugging Tools in the Linux Environment

To develop any software for the Cobalt module a good integrated development environment (IDE) is indispensable. A full-featured IDE such as Eclipse is recommended. It is necessary to configure the

IDE to use the ReadyFlow board support libraries, which greatly simplifies the task of using the board resources. Without such a tool, development work is a slow process and debugging a program can be extremely challenging without comprehensive knowledge of the Cobalt board and ReadyFlow.

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Appendixes

A – Controller Program `baseline_uct_demo.c`

This is an extract of the C-program which was used to do the waveform generation and digitization testing. Only sections which control the tuning frequencies and card operation are shown. Note that “// ...” denotes lines of code omitted for clarity, and “// !!” preceeds a description if what is being done in that code block.

```

/*****
*File:      baseline_uct_demo.c
/*****
#include "baseline_uct_demo.h"

// !! Parser function "handler" extracts experimenta parameters from a .ini file.
static int handler(void* user, const char* section, const char* name,
const char* value)
{
// ...
}

/*
*****
*Function:   main
*****
*/
int
main (int argc, char *argv[])
{
// ...
/*
*****
*initialize os independent library and install handler, create semaphore
*create filename if requested
*****

```

```

*/
// ...
/*
*****
*configure the 71621 board as a whole
*****
*/
// ...
/*
*****
*!! setup the DDC
*!! Load waveform from memory
*!! Setup the DUC
*****
*/
funcSetupDdcChannel(/* ... */);
funcLoadChirpWaveform(/* ... */);
funcSetupDucChannel(/* ... */);
/*
*****
*!! Start the main loop
*****
*/
// ...
funcSetGateSourceToExternal();
// ...
printf("\n\nWAITING FOR TRIGGER... \n\n");
while((strAtExit.wdExitFlag != TRUE))
{
// !! 1. Wait for trigger event.
// !! 2. When trigger is occurs, generate the waveform
// !!    and start digitization simultaneously.
// !! 3. Append the recorded information to "baseline_uct_demo.bin".
// !! 4. Reset the trigger to accept the next trigger pulse.
}

// !! Shut down the Cobalt module.
return 0;
}

/*
*****
*Function:      funcInitCmdlineDefaults
*Description:   Called to initialize the command line defaults in play
*               when user parameters are not specified

```

```

*****
*/
void
funcInitCmdlineDefaults(/* ... */)
{
ptrCmdParams->devType      = -1;
ptrCmdParams->clockFreq    = 360e6;
ptrCmdParams->xferSize     = DEFAULT_BUFFER_SIZE;
ptrCmdParams->interpolation= 2;
ptrCmdParams->decimation   = 2;
// The tuning frequencies for the DDC and DUC are set under the
// funcSetupDucChannel() and funcSetupDdcChannel() function definitions.
ptrCmdParams->tuneFreq      = 55.0e6;
ptrCmdParams->loop          = 0x00000001;

// !! Parser initialization
// ...
}

// !! Other function definitions.
// ...

```

B – RF loop-back recordings of 50MHz BW LFM Pulse

In this section the radio frequency signals generated in an IF loop-back test using the Cobalt Digital Transceiver and the REX are presented. In both cases the input signal was the standard 50 MHz bandwidth, LFM chirp pulse on the 125 MHz intermediate frequency carrier, generated by the Cobalt DAC channel A output. An Aglient E4407B ESA-E series spectrum analyzer was used to capture spectra at IF and RF frequencies.

Figures B.1 and B.3 show the RF spectra of signals generated by the REX. These are the upconverted baseband spectra. Looping back the RF outputs to their respective RF input channels of the REX produced downconverted IF spectra shown in Figures B.2 and B.4. The samples of the transmitted and received baseband pulses in these loop-back recordings are shown in Figures B.5 and B.6.

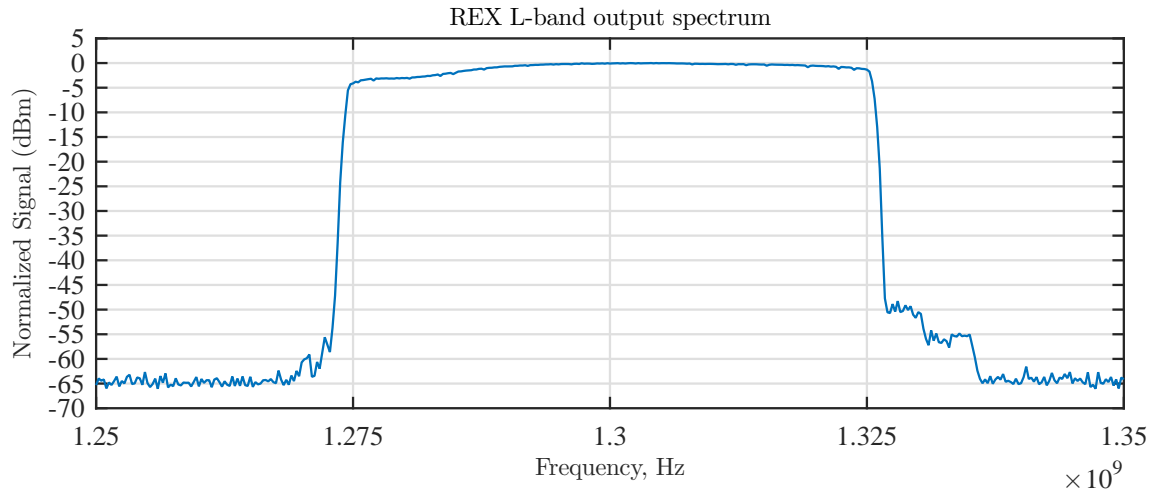


Figure B.1: L-Band 50 MHz bandwidth, LFM Pulse spectrum from REX upconverted from the Cobalt-generated IF signal.

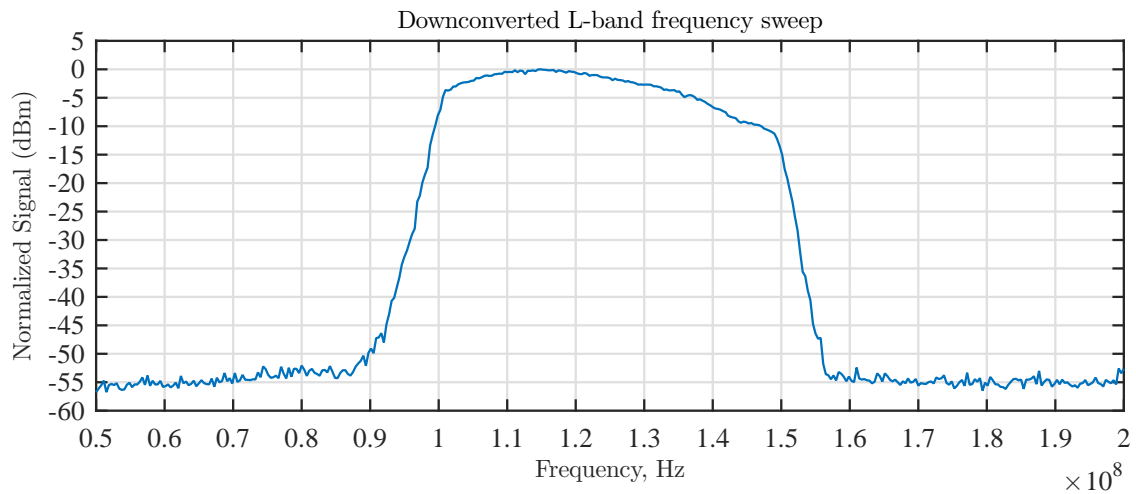


Figure B.2: L-band 50 MHz bandwidth, LFM pulse downconverted from RF to the 125 MHz IF.

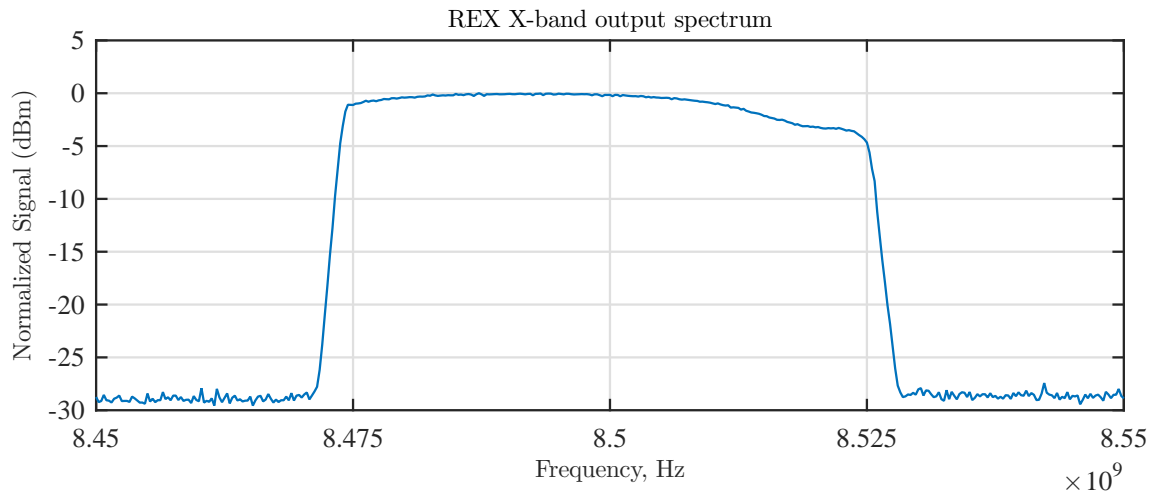


Figure B.3: X-Band 50 MHz bandwidth, LFM Pulse spectrum from REX upconverted from the Cobalt-generated IF signal.

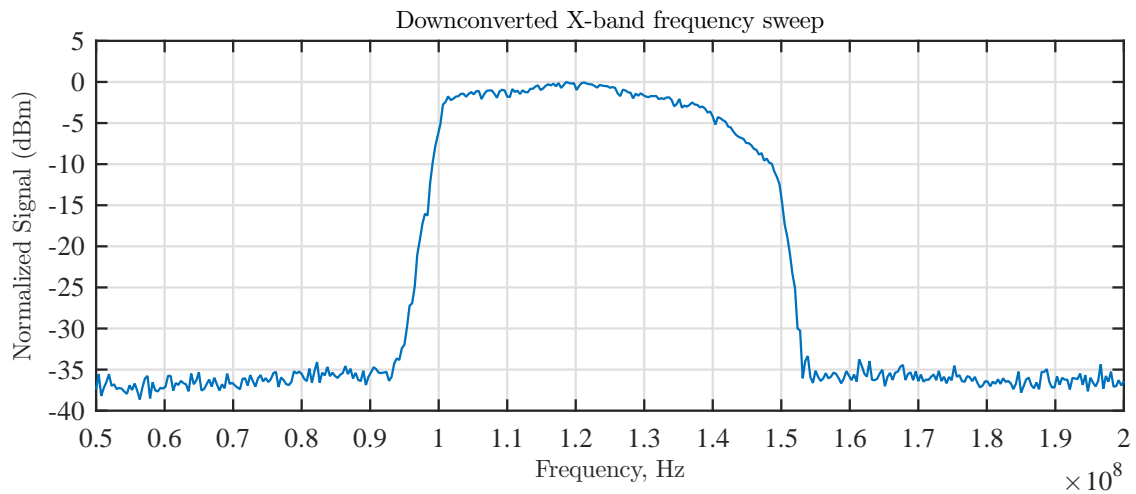


Figure B.4: X-band 50 MHz bandwidth, LFM pulse downconverted from RF to the 125 MHz IF.

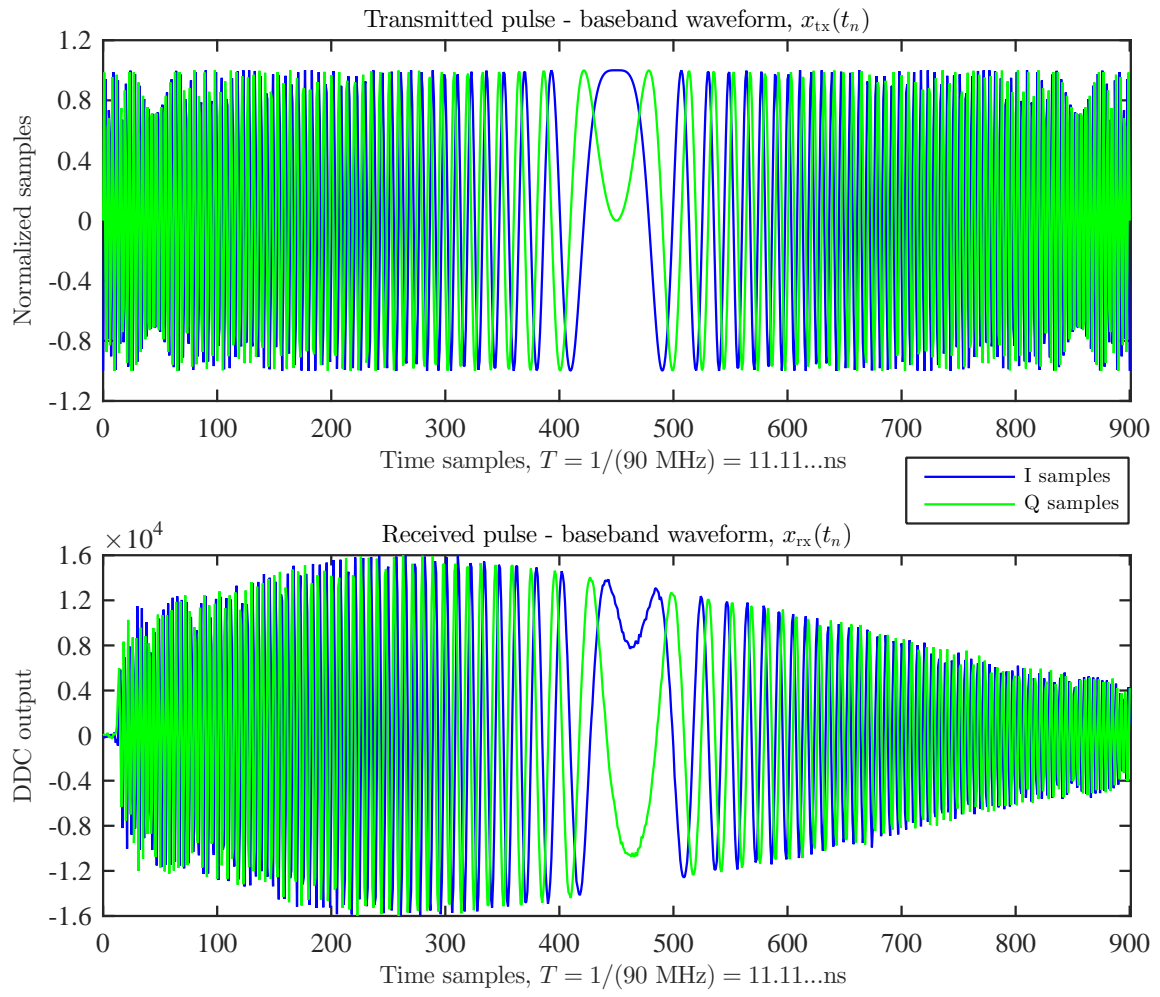


Figure B.5: Data samples in the L-band loop-back measurement.

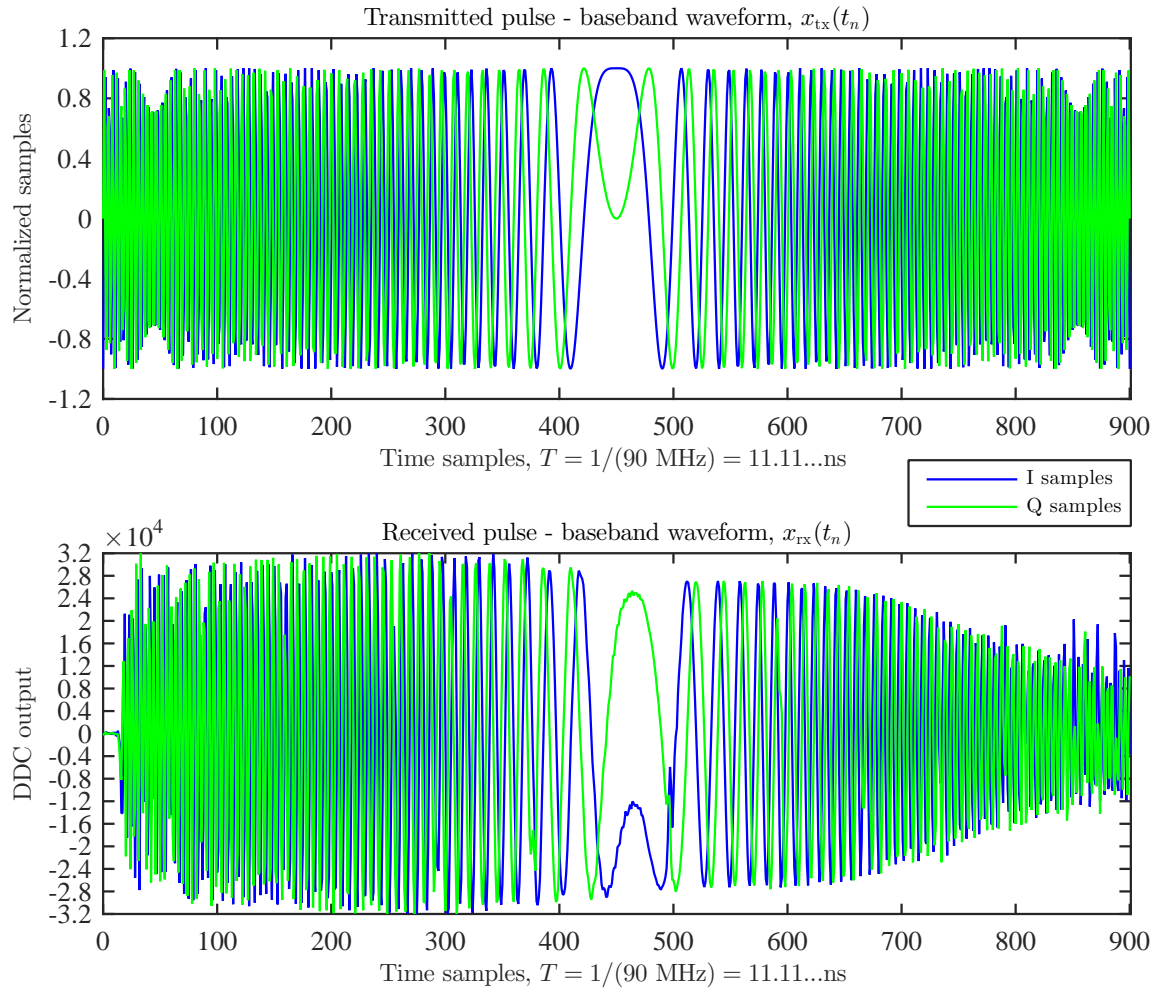


Figure B.6: Data samples in the X-band loop-back measurement.